Problem #1
Answer the following questions using the 90-nm CMOS technology provided. You are welcome to layout the structures in Cadence.
(a) What is the minimum PMOS diffusion length (L_{DIFF}) without contacts?
(b) Estimate the dimensions of a minimum sized transistor that has contacts on its diffusion. Be sure to account for gate extension in the direction of the width.
(c) What is gate extension and why is it there?
(d) What is the minimum metal1-to-metal1 pitch (center to center) with contacts/vias?
(e) What is the minimum metal9-to-metal9 pitch (center to center) with vias? Why is this different from (d)?
(f) What is the center-to-center pitch between the diffusion of a transistor? This is very useful in estimating the size of a layout.
(g) Explain why the parameters for the sidewall capacitance of a transistor are different from the bottom-plate capacitance of the source/drain diffusion. Often a channel facing side of the diffusion also has different parameters, why?

Problem #2
Draw the switch logic for the following logical function, assume that true and complement inputs are available. Use the fewest number of switches.
(a) f = (a + b')c
(b) f = a xor b xnor c

Problem #3
What is the steady-state voltage (assuming no subthreshold current) for each of the following scenarios. You can assume that V_{TN}=-V_{TP}=0.2V.

Problem #4
Determine the final voltages for all nodes for each of the scenarios below. Assume that V_{TN}=-V_{TP}=0.25V.