MOS Device Modeling

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Courtesy of Agilent eesoft
Overview

• Reading
  – Rabaey 3.3
  – W&H 2.2-2.4

• Overview
  – This class will look at the iV and CV characteristics of an MOS device in more detail to try to explain some of the limitations of the simple RC models that we observed in the previous lecture, and to give us some insight about how the simple RC models will change when we change power supply voltages or technology. We will extend the quadratic model to handle effects in a modern technology. In these lectures we will define a ‘magic’ threshold voltage where the transistor starts to conduct, and describe briefly how this threshold depends on operating parameters. Later in the class we will revisit the issue of threshold voltage.
Review: Equation w/ Saturation

- If we clamp the equation we get:

\[ I_{ds} = \frac{W}{L} \mu C_{ox} \left( \frac{V_g - V_s - V_{th} - \frac{V_{ds}^*}{2}}{2} \right) V_{ds}^* \]

\[ V_{ds}^* = \min \left( V_{ds}, V_g - V_s - V_{th} \right) \]

- There is no current variation with output voltage
\( i_{ds} \) as Function of \( V_{ds} \)

- Several mechanisms
  - Channel Length Modulation (CLM)
  - Drain Induced Barrier Lowering (DIBL)
  - Substrate Current Body Effect (SCBE)
- The dominant effect for digital circuits is CLM
  - As the drain voltage rises above \( V_g - V_{th} \), there is a high-field region (\( E_{max} \)) that forms to drop this excess voltage at the drain end of the channel.
  - While the E-field is high, it is not infinite (\( E_{max} \sim v_{sat}/u_{eff} \)), so it takes a finite distance to drop this voltage. The net result is that the “channel length” is a function of the drain voltage when the transistor is saturated.
  - The “channel” is effectively shortened.
- The effect is also known as finite output impedance, \( r_o \).
Aside: Incremental Resistance

- Often measure the **small-signal** resistance
  - What is the effective resistance at this operating point
  - Usually measured in conductance, rather than resistance

- Two important conductance values for MOS drain current
  - $g_m =$ change in drain current when you change $V_{gs}$
    - $\frac{di_{ds}}{dV_{gs}}$
  - $g_{ds} =$ change in drain current with a change in $V_{ds}$
    - $\frac{di_{ds}}{dV_{ds}}$
    - In the saturation region, $1/g_{ds} = r_o$.
  - Both are a function of DC operating point of $V_{gs}$ and $V_{ds}$. 
Modeling CLM

- Simple model:

\[ L_{\text{eff}} = L_{\text{elec}} - \zeta (V_d - V_c) \]

\[ i_{\text{dsat}} \approx \frac{W}{L_{\text{elec}}} \mu C_{\text{ox}} \left( 1 - \frac{\zeta (V_d - V_{\text{dsat}})}{L_{\text{elec}}} \right) \left( \frac{1}{2} \right) (V_{gs} - V_{th})^2 \]

\[ i_{\text{dsat}} \approx \frac{W}{L_{\text{elec}}} \mu C_{\text{ox}} \left( \frac{1}{2} \right) (V_{gs} - V_{th})^2 \left( 1 + \frac{\zeta (V_d - V_{\text{dsat}})}{L_{\text{elec}}} \right) \]

- Observations
  - CLM is a function of the length of the channel \((L_{\text{elec}})\)
  - \(r_o\) is worst for higher \(i_{\text{dsat}} (V_{gs})\)
  - \(\zeta L_{\text{min}}\) is approximately 0.1-0.4
  - \(\zeta\) is not a linear function of \(V_{ds}\) (sublinear)
  - \(\zeta\) is a function of \(E_{\text{max}}\) (a function of \(u_{eff}\))
CLM Model Results

- Results in higher currents.
  - 90nm gpdk results in almost 20% more current than the current at $V_{\text{dsat}}$.
  - Good for digital applications (higher $I_{\text{on}}$)
Aside: Output Impedance Factors

- Plot is biased at $V_{gs} \sim 2V_{th}$
Aside: Drain-Induced Barrier Lowering

- For short channel lengths, $V_d$ can result in 2-D E fields in the silicon
  - Causes the conduction barrier to be lowered at the source side
- Effectively reduces the threshold voltage
- Depends on the ratio of the channel length to the depth of the source and drain junctions.
  - Shallow junctions reduces DIBL.
Aside: Modeling DIBL

- A simple formula is:
  - Where $\xi = 0.02$ to $0.1$

\[
V_{th} = V_{th0} - \xi (V_{ds})
\]

\[
i_{dsat_{DIBL}} \approx \frac{\mu C_{ox} W}{2 L_{eff}} (V_{gs} - V_{th0} + \xi V_{ds})^2
\]

\[
\frac{\partial i_{ds}}{\partial V_{ds}} \approx \frac{\mu C_{ox} W}{L_{eff}} (V_{gs} - V_{th0} + \xi V_{ds}) (\xi)
\]

- Observations
  - Smaller effect at high $V_{gs}$
  - Very strong effect in subthreshold.
Aside: Substrate Current Body Effect

- High electric field at the Drain causes electrons to be highly energetic, “hot”
  - Impact (w/ silicon) ionization causes hole/electron pairs.
  - Substrate-drain current
  - Need $V_{ds} > 1.5V$
Modified Effective Resistance

\[ V_{GS} \geq V_T \]

\[ R_{on} \]

\[ S \rightarrow \text{X} \rightarrow D \]

\[ \zeta = \lambda L_{\text{min}} \]

\[ R_{\text{eff}} \approx \frac{1}{2} \left( \frac{V_{DD} \left( 1 - \frac{\lambda L_{\text{min}}}{L_{\text{elec}}} \right) V_{DD}}{I_{\text{DSATN}}} + \frac{(V_{DD}/2) \left( 1 - \frac{\lambda L_{\text{min}}}{L_{\text{elec}}} \right) (V_{DD}/2)}{I_{\text{DSATN}}} \right) \]

\[ R_{\text{eff}} \approx \frac{3}{4} \frac{V_{DD}}{I_{\text{DSATN}}} \left( 1 - \frac{5}{6} \left( \frac{\lambda L_{\text{min}}}{L_{\text{elec}}} \right) V_{DD} \right) \]
Effective Current

\[ I_{\text{eff}} \approx \frac{1}{2} (I_{\text{max}} + I_{\text{mid}}) \approx I_{\text{ds}} \left( V_{\text{gs}} = V_{\text{dd}}; V_{\text{ds}} = \frac{3}{4}V_{\text{dd}} \right) \]

\[ I_{\text{eff}} = \frac{W}{L_{\text{eff}}} \mu C_{\text{ox}} \left( \frac{1}{2} \right) \left( V_{\text{gs}} - V_{\text{th}} \right)^2 \]

\[ L_{\text{eff}}^* = L_{\text{elec}} \left( 1 - \frac{\lambda L_{\text{min}} \left( \frac{3}{4}V_{\text{dd}} - V_{\text{dsat}} \right)}{L_{\text{elec}}} \right) \]

\[ \text{delay} = C \Delta V/I_{\text{avg}} \]

\[ \zeta = \lambda L_{\text{min}} \]
Bulk Charge Effect

- $V_{th}$ changes with $V_c$
- There is an easy fix for this problem.
  - Assume that $V_{th}(V_c)$ is a linear function
    - First order approximation
    - $V_{th} = V_{tho} + \delta V_c$
  - Can be easily handled

\[
Q_n = -C_{ox} \left( V_g - V_c - V_{th} - \delta V_c \right) = -C_{ox} \left( V_g - V_c (1+\delta) - V_{th} \right)
\]

\[
\int i_{ds} \, dy = \int W \mu C_{ox} \left( V_g - V_c (1+\delta) - V_{th} \right) dV_c
\]

\[
i_{ds} = W \mu C_{ox} \left( V_g - V_s - V_{th} - \left(1+\delta \right) \frac{V_{ds}}{2} \right) V_{ds}
\]
The model is looking better but still the wrong shape.

It matches well at low $V_{gs}$, and even at moderate $V_{gs}$ and low $V_{ds}$, but does not match at all at high $V_{gs}$.

The model has too much current.

Cannot be fixed by scaling the current in the model (making mobility smaller).
0.35um pMOS Comparison

- Not as bad as nMOS device. The shape seems roughly right.
- Still have trouble matching the current
- Clearly the mobility is not constant!
Modern Transistor

- Unfortunately this modified quadratic model is pretty old

- Transistors I-V does not look like that any more
  - To get higher performance E-fields have gone up
  - Both vertical gate field ($V_{gs}/t_{ox}$)
  - And lateral field ($V_{ds}/L$)

- Under high fields, mobility is not constant
  - High gate (vertical) E-field reduce the effective mobility
  - Carriers have a max velocity, $v_{sat} = 10^7\text{cm/s}$

- This causes $i_{ds} = (V_{gs} - V_{th})^{\alpha}$,
  - where $\alpha$ is about 1.25
High-Field Effects
Overview

• Reading
  • Rabaey 3.3

• Overview

Today we will first look at the effect that high-fields have on a transistor. High fields have two principle effect -- to make the threshold voltage a function of the device dimensions, and to reduce the current through the device by limiting the carrier velocity. The book has a large discussion of the short-channel threshold effects. While it is important to realize that the threshold depends on device geometry, remembering the exact formulas is not needed. Some of today's devices have ‘reverse short channel’ effects. The part to focus on is the effect of velocity saturation, and the modeling of the charge storage in a transistor
Real Transistors

• Current is less than projected by first order model
• Main error is in the approximation for mobility
  – Assumed that it was a constant
  – Really it is affected by both vertical and horizontal fields

• For the linear region
  – Vertical field effect is most important

• For the saturation current
  – Horizontal field and velocity saturation dominate

There are adjustments to the models that we can use
Mobility Degradation

- (left): 30+\% mobility reduction due to carriers pulled to collide with the surface.
- (right) Linear region plot of the current
nMOS Vertical Field

- Primarily reduces the conductance in the linear region

\[ \mu \cdot e(V_{gs}) := \frac{540}{V_{gs} + V_{th}} \left( 1 + \frac{V_{gs} + V_{th}}{t_{ox} \cdot 0.54 \cdot 10^3 \frac{V}{\mu m}} \right)^{1.85} \frac{cm^2}{V \cdot s} \]

- For a 0.35-\(\mu m\) transistors, \(T_{ox} = 7.3\) nm, \(V_{gs} + V_{th} = 4\)

This is an empirical formula that was derived from data taken by the Berkeley device group headed up by Dr. Hu. The paper reference is IEEE Trans on Elect. Dev, Nav 97, “Predicting CMOS Speed with Gate Oxide and Voltage Scaling and Interconnect Loading Effects”, Kai Chen et. al.
pMOS Vertical Field

- Reduces mobility but the fitting parameters is a little different,

\[
\mu_h(V_{gs}) := \frac{185}{1 + \left[ \frac{V_{gs} + 1.5 \cdot V_{th}}{t_{ox} \cdot 0.75 \cdot 10^3 \frac{V}{\mu m}} \right]} \cdot \frac{1}{\cdot \frac{1}{.45}} \cdot \frac{cm^2}{V \cdot s}
\]

- BSIM4 uses an even more complex model for both devices

\[
\mu_{eff} = \frac{U_0}{1 + (UA + UC \cdot V_{bseff}) \left( \frac{V_{gseff} + C_0 \cdot (V_{TH0} - V_{FB} - \Phi_s)}{TOXE} \right) EU}
\]
Velocity Saturation

- We have been assuming as the carriers density goes down, the electric field goes up, and the carriers move faster
- Carriers (e-) cannot move faster than $8 \times 10^6$ cm/sec = $v_{sat}$
  - Current saturate when $C_{ox}(V_{gs} - V_{th} - V_{ds}) v_{sat} = i_{ds}$
  - Unlike before, carriers are hitting $v_{sat}$ before $V_{ds} > V_{gs} - V_{th}$
Velocity Saturated Transistors

• There are many ways to calculate the i-V curves
  – They all give similar results
  – I will use the one that gives the simplest results
  – But it is a little tricky
    • Journal Solid State Circuits, Aug 88, Toh, Ko, Meyer
    • pg 950-958
• Approximate mobility
  – Piecewise linear
  – Use effective mobility
    • reduced by vertical field
    • Critical field depends on $V_{gs}$

\[ v = \frac{\mu_e E}{1 + \frac{E}{E_c}} \quad E \leq E_c \]
\[ v = v_{sat} \quad E \geq E_c \]
\[ E_c = \frac{2v_{sat}}{\mu_e} \]
Critical Field

- Since the mobility depends on the gate field, the $E_c$ also depends on $V_{gs}$.
  - Often choose $E_c$ at $V_{gs}=V_{dd}$ for simplicity and worst case degradation.
• Solid lines are the real electron velocity for two different gate voltages (3V, and 1V), the dotted lines are the model, and the green dotted line is the model for pMOS. Velocity saturation is less of an issue for pMOS devices.
Modified i-V Equations (1)

\[ i_{ds} = W Q \frac{V}{W} = WC_{ox} (V_g - V_c - V_{th}) \frac{\mu \frac{E}{V}}{1 + \frac{|E|}{E_c}} \]

\[ i_{ds} = W \frac{\mu \frac{E}{V}}{1 + \frac{|E|}{E_c}} C_{ox} (V_g - V_c - V_{th}); \text{ but } E = \frac{dV_c}{dy} \]

rearranging terms and noting that \(|E|\) is \(-E\)

\[ i_{ds} = W \mu \left[ C_{ox} (V_g - V_c - V_{th}) + \frac{i_{ds}}{W \mu \frac{E}{V}} \right] \frac{dV_c}{dy} \]
Modified i-V Equations (2)

\[ i_{ds} = \frac{W}{L} \frac{\mu_e C_{ox}}{1 + \frac{V_{ds}}{E_c L}} \left( V_g - V_s - V_{th} - \frac{V_{ds}}{2} \right) V_{ds} \]

Saturation occurs when the current forces the carriers at the end of the channel to move at \( v_{sat} \)

\[ i_{ds} = Wv_{sat} C_{ox} \left( V_{gs} - V_{th} - V_{ds} \right) \]

Equating these two equations lets one solve for \( V_{dsat} \), and the current in saturation. It takes lots of math, but gives:

\[ V_{dsat} = \frac{\left( V_{gs} - V_{th} \right) E_c L}{\left( V_{gs} - V_{th} \right) + E_c L} \]

\[ i_{dsat} = Wv_{sat} C_{ox} \frac{\left( V_g - V_{th} \right)^2}{\left( V_{gs} - V_{th} \right) + E_c L} \]
Modified i-V Equations (3)

- Incorporating CLM
  - Use the $L_{\text{eff}}$ instead of $L$
  - But the equations gets a little tricky because $L_{\text{eff}} = f(V_{\text{dsat}})$
- To estimate drive current ($V_{\text{gs}} = V_{\text{dd}}$)
  - Estimate $V_{\text{dsat}}$ using $L = L_{\text{elec}}$ (the electrical channel length)
  - Calculate effective current using $L_{\text{eff}}^*$

$$V_{\text{dsat}} = \frac{(V_{\text{gs}} - V_{\text{th}})E_c L_{\text{elec}}}{(V_{\text{gs}} - V_{\text{th}}) + E_c L_{\text{elec}}} = \frac{(V_{\text{gs}} - V_{\text{th}})}{1 + \frac{V_{\text{gs}} - V_{\text{th}}}{E_c L_{\text{elec}}}}$$

$$L_{\text{eff}}^* = L_{\text{elec}} \left(1 - \frac{\lambda L_{\text{min}} \left(\frac{3}{4} V_{\text{dd}} - V_{\text{dsat}}\right)}{L_{\text{elec}}}\right)$$

$$i_{\text{dsat}} = \frac{W}{2L_{\text{eff}}^*} \frac{\mu_e C_{\text{ox}}}{\left(1 + \frac{V_{\text{gs}} - V_{\text{th}}}{E_c L_{\text{eff}}^*}\right)} \left(V_{\text{gs}} - V_{\text{th}}\right)^2$$
i-V Discussion

- $V_{\text{dsat}}$ is not fixed, except since mobility decreases with increase $V_{gs}$, $V_{ds}$ increases to compensate.
- $I_{\text{dsat}}$ is initially quadratic, but then becomes linear.
- $I_{ds}$ equation has a good feel to it:
  - Correct in both limits
    - Complete velocity saturation
      - Current linear on voltage
    - No velocity saturation
      - Becomes quadratic model
- Key parameter is the relation of $E_cL$ to $V$
  - In a $L = 0.4\mu$ technology
    - $E_c = 6V/\mu$; $E_cL = 2.4V$
  - $V_{gs} - V_{\text{th}} = 3\text{ish}$;
Model Comparison

- Not perfect, but not terrible either
Aside: Alpha-Power Model

- Simplified equation for current scaling
  - Chen in Transactions in Electron Devices Nov 97 presented a simple model of $i_{\text{dsat}}$ for scaling. His model was based on alpha-power law.
  - Clearly current is not quadratic on $(V_{gs}-V_{th})$, so try to match it to some power.

\[
I_{\text{dsat}} = k_c W (V_{gs} - V_t)^\alpha
\]

\[
V_{\text{dsat}} = k_v (V_{gs} - V_t)^{\alpha/2}
\]

- Today’s devices, the power is roughly 1.25
  - If we focus on the current equation (within a couple of generations of 0.25um)
  - $i_{ds} \propto L^{-0.5} T_{ox}^{-0.8} (V_{gs}-V_{th})^{1.25}$
Impact of Temperature

Changing the temperature changes the device currents

- Increasing T makes $V_{th}$ smaller in magnitude.
  \[ V(T) = V(T_{ref}) - k_{VT} (T - T_{ref}) \]
  \[ k_{VT} = 0.5 - 3\text{mV/K} \]

- Mobility
  - Mobility also proportional to $(T/T_o)^{-3/2}$
    - $k_\mu$ is between -1.2 and -2
    - T is in Kelvin
  - 30% slower significant change from 27-100°C
  - $\nu_{sat}$ does not change that much

\[ \mu(T) = \mu(T_{ref})(\frac{T}{T_{ref}})^{k_\mu} \]
Impact of Series Junction Resistance

- Less deep junction improves DIBL, but...
- Source and drain resistances are becoming comparable to channel resistance. 25% at 65nm technology.
Geometry Effects: Short/Narrow Channel

- $L_{eff} = L - \Delta L$
  - Reduced L (design) results in larger $\Delta L$
  - Increases current
- Opposite is true for narrow width
i-V Summary

- The basic quadratic model is no longer sufficient
  - Short channel lengths and higher electric fields creates a myriad of effects and problems
  - Many result in reduced $I_{on}$
    - Mobility degradation, velocity saturation, junction resistance
    - And increased $I_{off}$ (as we will see later)
  - Causes the Elmore delay model to not be as effective
    - Must treat P/NMOS networks as an effective resistance/current.
- Many possible models
  - Physically based model
  - Alpha-power simple fitted model
  - BSIM3 is a blend and accounts for all effects (including $T$).
    - Many fitting parameters, and similar general form
Capacitance
Review: Charge Storage Basics

- Three basic capacitance to worry about:
  - Wiring, is usually the largest
    - Discuss more later, but is a nice linear capacitor
    - Often couples things you don’t want coupled
  - Junction
    - Non-linear cap, simple geometry
  - Gate
    - Non-linear capacitance to model channel
Review: MOS Model

- $C_1$ - $C_4$ - gate capacitances
- $C_j$ -- are junction capacitances
Gate Overlap (\(C_1, C_3\))
- Two terms
  - \(C_{ox} W L_D = \) true overlap
  - \(C_{gso}, C_{gdo} = \) fringe cap off the side of the gate
- In modern devices \(L_D\) is very small (spacers)
- But you still have the fringe field
  - \(0.2fF/\mu\) for each edge
Review: Junction Cap

- Three geometry-dependent pieces
  - Bottom
    - Area capacitor, proportional to $W_{\text{eff}} \times \text{DiffExt}$
  - Sidewalls
    - Edge capacitor, proportional to $(W_{\text{eff}} + 2 \times \text{DiffExt})$
  - GateEdge
    - Edge capacitor for the junction edge under the transistor
    - Included in the SPICE model,

\[ \text{DiffExt} \]
Review: Junction Capacitance

- Plot shows the cap is not linear
  - Each junction has three components
    - Area, outside edge and gate edge
    - Edge are important
  - In SPICE model
    - Area $C = C_j (V_{bs}+2\phi)^{m_j} \times AS$
    - Perm $C = C_{jsw} (V_{bs}+2\phi)^{m_{jsw}} \times PS$
    - Gate Edge = $C_{jgate} (V_{bs}+2\phi)^{m_{jsw}} \times W$
Review: Channel Charge

- Traditional derivation shows that the channel charge changes with the region of operation.
Review: MOS Capacitance Table

- The capacitance for channel charge is often summarized in a table

<table>
<thead>
<tr>
<th>APPROXIMATE</th>
<th>OFF</th>
<th>LINEAR</th>
<th>SATURATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{GS}$</td>
<td>$C_1$</td>
<td>$C_1 + \frac{1}{2} C_2$</td>
<td>$C_1 + C_2$</td>
</tr>
<tr>
<td>$C_{GD}$</td>
<td>$C_3$</td>
<td>$C_3 + \frac{1}{2} C_2$</td>
<td>$C_3$</td>
</tr>
<tr>
<td>$C_{GB}$</td>
<td>$\leq C_2$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$C_{GB}$</td>
<td>$&gt; 1/(1/C_2 + 1/C_4)$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$C_{SB}$</td>
<td>$C_{jSB}$</td>
<td>$C_{jSB} + \frac{1}{2} C_4$</td>
<td>$C_{jSB} + \frac{2}{3} C_4$</td>
</tr>
<tr>
<td>$C_{DB}$</td>
<td>$C_{jDB}$</td>
<td>$C_{jDB} + \frac{1}{2} C_4$</td>
<td>$C_{jDB}$</td>
</tr>
</tbody>
</table>
Accounting For Channel Charge

- For quadratic model, get 2/3 of $C_{ox}$ when transistor is in sat
- For velocity sat device, it will be more than 2/3
  - $V_{dsat}$ is lower

- **It is easier just to use $C_{ox}$**
  - This is a small cap, and error will be small
  - Also, in a digital gate, the transistor ends in linear region so you need eventually to supply $C_{ox}V$ charge
    - Actually the charge is $C_{ox}(V_{dd} - V_{th})$
Short/Long Channel Charge

- Capacitance asymptotically approach 0 (off), $1/2$ (linear), and $2/3$ (saturation) as we sweep $V_{DS}$ for various $V_{GS}$.
  - Only true for long channel.
  - $C_{OV}$ is significant enough to be $1/5$ of total $C$. 
Dealing with Nonlinear Capacitance

• Linear capacitor
  – \( Q = CV \)

• Nonlinear capacitor
  – \( C(V) \)
  – Regions of operation

• Small signal approximation

• Large signal approximation
  – Hand calculation uses a “\( C_{eq} \)”
    • Equivalent linear capacitor
  – Average \( \Delta Q \) for a \( \Delta V = V_{dd}/2 \)

• This explains why the effective linear cap rising and falling transitions are different. The voltage range for the capacitor for delay are different (\( V_{dd} \) to \( V_{dd}/2 \) or \( V_{dd}/2 \) to Gnd) so the average value of capacitance in these regions is slightly different.
Effective Capacitance

• We used a simulator to find effective capacitances
  – Simulate inverter with real non-linear capacitance
  – Simulate inverter with linear cap
  – Find linear cap that matches the delays
• These methods work well, but need to remember that capacitance values are
  – For the voltage range you used.
  – For different transitions.
    • Different coupling
Simple Capacitance Insights

• The capacitance of a MOS device is not linear
  – Can use this fact to your advantage
  – (And explains some anomalies)
• Junction capacitance
  – Decreases with increasing voltage
    • Depletion depth increases
  – If you have a large number of nMOS source/drains on a line
    • It is good if the line is at Vdd (lowest incremental cap)
    • Better if you only swing line a small amount
    • Adding substrate voltage reduces cap more
    • Rising and falling delays will not match!!
Impact of Nonlinear Gate Capacitance

• The nonlinearity of the gate capacitance will effect our delay as well.
  – Until the transistor ‘turn on’ the gate capacitance is smaller
  – If pMOS are 2x nMOS, then cap when input is near Gnd will generally be larger than cap when input is near Vdd, since near Gnd nMOS are off, while near Vdd the pMOS are off.
  – This will effect rising and falling delay
    • In particular be careful if you try to find the right ratio of nMOS to pMOS devices by matching delays. The result will depend on whether you use a linear cap, or an inverter as a load

• A significant fraction of the capacitance is overlap capacitance
  – Does not depend on voltage – a “linear” capacitance
  – Causes delay to depend on loading on the successor gate.
  – Causes all kinds of interesting effects in amplifiers
Miller Capacitance (Small Signal)

KCL at amplifier input:

\[ I_{in} = \frac{V_{in}(1+A)}{1 + sC} = V_{in}(1+A)sC \]

- Input impedance = \( \frac{V_{in}}{I_{in}} = \frac{1}{sC(1+A)} \)
- The capacitor value \( C \) is multiplied by \( 1+A \) !!

Courtesy of MG Johnson
Miller Effect in Logic Gates

- Node C is unloaded, node Y load = FO4
  - Node C switches hi very quickly, much faster than node Y
  - This puts a huge $\Delta V/\Delta t$ across $C_M$, causing a large $I_M$
  - Inverter G2 must “swallow” the extra $I_M$
    - Which slows down node B

Courtesy of MG Johnson
Simple Large Signal Approximation for Miller Effect.

• Consider the full swing of the input.
  – The effective $\Delta V = 2V_{dd}$ so $\Delta Q = 2V_{dd}C_{eq}$
  – Equivalent capacitance is $2C_{eq}$
• Model this by doubling the input and output overlap capacitance.
  – Does not account for the waveform shape
  – Extra charge may not impact delay… will impact power

![Diagram of transistor circuit with Miller capacitance approximation]
Impact on Signal Waveform

Node B drives Miller-multiplied capacitance CM

 Courtesy of MG Johnson
Possible Transition Scenarios

- Many possible transitions are possible.
- May need to create a table of different cases.
- First 3 cases are most common.

Courtesy of W&H
C-V Summary

• Devices are small enough that we primarily are concerned with the capacitance between terminals
  – RF models include distributed capacitance (BSIM4)
• Models are generally linear
  – Nonlinear junction caps (sqrt relations)
    • Can take advantage of this effect in design
  – Device capacitance across regions of operations (dominated by linear parasitics)
• Complexity is the coupling between the many nodes
  – Can lead to errors in delay/power estimates
  – Causes denser coupling matrices and hence computational complexity.