Design and Reliability of a Micro-Relay Technology for Zero-Standby-Power Digital Logic Applications
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Abstract

Micro-electro-mechanical (MEM) relays recently have been proposed for ultra-low-power digital logic applications because their ideal switching behavior may allow for further supply-voltage (VDS) scaling [1-3]. This paper describes design techniques to achieve reliable (high-endurance) MEM relay operation. Prototype relays fabricated using a CMOS-compatible process are demonstrated to operate with low surface adhesion force, adequately low on-state resistance (RON < 100kΩ) over a wide temperature range (20°C-200°C), and >10⁶ on/off switching cycles in N₂ ambient without stiction- or welding-induced failure. Measured characteristics are well predicted by both ANSYS simulations and analytical models. Using the calibrated analytical model, a scaled relay technology is projected to operate at VDS < 1V and provide >10x energy savings for circuits operating at up to ~100MHz.

Introduction

The principal challenge facing microrelay designers is achieving good reliability while maintaining sufficiently low contact resistance. Because the on-state conductance of a microrelay is limited by asperities on the contacting metallic surfaces, soft contacting electrode materials (esp. gold) are used for radio-frequency signal DC switching applications, which require extremely low RON (<1mΩ). Furthermore, a large load is applied to plastic deform [4-7] the contacting surfaces such that the metallic material liquefies. However, this makes high endurance very difficult to achieve with such designs [6]. In contrast, for digital logic applications, RON can be as high as 10-100kΩ (for load capacitance of 10-100fF) because the switching delay of a relay-based circuit is dominated by the mechanical pull-in time (tPI, typically 10-100ns) rather than the electrical RC delay (tRC) [1]. Since extremely high endurance is a necessity in this application while relatively high RON can be tolerated, hard contacting electrode materials [8-10] (e.g. tungsten) and operation with low contact force [8] are preferred. In addition, a surface treatment can be applied to reduce adhesion [9,11] as long as RON is not increased beyond ~100kΩ. With these considerations in mind, we have developed a reliable relay technology suitable for digital logic applications using titanium dioxide (TiO₂) coated tungsten (W) electrodes. The TiO₂ coating is hydrophobic [12], and therefore "stiction" due to water-mediated adhesion is avoided [11]. TiO₂ is also a high electron affinity dielectric (QFE/W=4.2eV), and thus presents only a moderate potential barrier to electron conduction from W, i.e. it degrades on-state conductance least among common dielectric materials.

Device Fabrication

The fabricated micro-relay structure and operation are illustrated in Fig. 1 and 2, respectively. Three-terminal relays were chosen for these experiments due to process simplicity, but the design techniques and results are equally applicable to other logic relay designs [1-3]. Relays with parameters shown in Table I were fabricated on oxidized Si wafer substrates as follows. Amorphous silicon (which promotes adhesion of W to SiO₂) and W layers, each 50 nm thick, were sequentially deposited by sputtering and then patterned to form the drain and gate electrodes (Fig. 3a). 100nm-thick LTO was then deposited at 400°C as the first sacrificial layer. Contact dimple regions were then formed by optical lithography and dry etching (Fig. 3b). After the deposition of a 2nd 100nm-thick LTO sacrificial layer (Fig. 3c), a 50nm-thick W layer was sputtered and patterned to form metallic contacting electrodes (Fig. 3d). Next, a 1μm-thick structural layer of in-situ boron-doped polycrystalline Si₃N₄Ge₀₁₆ was deposited at 410°C [13]. The Si₃N₄Ge₀₁₆ layer was then patterned (Fig. 3e) and the structures were released (Fig. 3f) with a timed isotropic oxide etch using vapor 49% hydrofluoric acid at 27°C. Immediately afterwards, the entire relay structure was coated with TiO₂ at 275°C using 12 cycles of atomic layer deposition (ALD). One ALD cycle consists of one pulse of titanium tetrachloride (TiCl₄) followed by Ti oxidation, and deposits ~0.25Å of TiO₂. Note that since the maximum process temperature is 410°C, this relay technology is suitable for fabrication over CMOS circuitry [14] or on glass substrates.

Results and Discussion

Fig. 4 shows a plan-view scanning electron micrograph (SEM) of a fabricated relay. All measured relays (>200) were found to be functional. Measured tPI-VON and tPI-VDS characteristics are plotted in Fig. 5. As expected, the relays have zero off state drain-to-source and gate leakage currents. Abrupt switching is seen at VON=5.35V and RON=8.1kΩ. Since the relay is operated in the pull-in mode, hysteretic switching behavior is observed. Both the pull-in VPI and the release voltage VRL voltages values well match ANSYS simulation results (Fig. 6), decreasing with increasing beam length (L). Analytically, VPI and VRL can be calculated as [15]:

\[
V_{PI} = \sqrt{\frac{4k_{eff}g_{d}^{2}}{27\varepsilon_{A}}} \quad V_{RL} = \sqrt{\frac{1}{2\varepsilon_{A}} (g_{d}-g_{a})^{2}} \quad \text{for } g_{d} > g_{a}.
\]

where k_{eff} is the effective spring constant that consists of flexural (∝1/L³) and torsional (∝1/L⁵) stiffness terms (Fig. 7, 8):

\[
\frac{1}{k_{eff}} = \left( \frac{3.66 \times 10^{13}}{E_{W}^{2}L} \right)^{-1} + \left( \frac{3.141 \times 10^{8} \times 2\times 10^{13}}{E_{W}^{2}L} \right)^{-1}.
\]

The surface adhesion force F_s is dominated by the metal-to-metal contacts; it can be estimated by expressing VRL as a function of VPI:

\[
V_{RL}^{2} = \frac{2g_{a}}{g_{d}} \left( 1 - \frac{g_{a}}{g_{d}} \right)^{2} V_{PI}^{2} - \frac{2g_{a}^{2}g_{d}^{2}}{\varepsilon_{A}}.
\]

The average F_s is extracted (Fig. 9) to be 0.45μN for a dimple area (A_D) of 2×10μm², with individual relays’ extracted F_s varying by ±1μN around this value.

Due to the serpentine spring design, the relay is robust against thermal stress effects, so that the measured values of VPI, VRL and RON do not significantly change with temperature (Fig. 10 and 11).

Fig. 11. tPI measurements were taken in N₂ ambient using the test setup shown in Fig. 12. tPI depends on VDI and k_eff (Fig. 13), as expected. No contact bounce is observed. The measured tPI data matches predictions using the lumped parameter model [16] within 20%, with an extracted quality factor value Q = 0.3. tPI-300ns for VDI=1.5VPI. The effective mass of the structure is estimated using ANSYS: m_eff=1.43µlbh/3.83µWh, where the 2nd term is due to the loaded-mass from the spring.

Endurance was studied using a similar test setup (with RON=0Ω). The relay can endure 1.25 billion on/off hot switching cycles (Fig. 14) with VDI=1V in N₂ ambient without stiction- or welding-induced failure. Further measurements are underway to characterize additional devices and investigate sources of contact resistance variation.

Relay Scaling and Energy Efficiency Limit

In order to reduce VDS, the dimensions of a relay must be scaled down into the sub-micron regime [1]. Ultimately, VDI scaling will be limited by the need to overcome surface adhesion energy (Γ) in order to break physical contact: 0.5k_{eff}g_{d}² ≥ Γ. This gives V_{DI,min} = V_{PI,min} = \sqrt{\frac{4g_{d}^{2}}{27\varepsilon_{A}}} \quad \text{and } E_{min} = CV_{DI,min} = \frac{1}{2\varepsilon_{A}} \left( \frac{1}{g_{d}} - \frac{1}{g_{a}} \right)^{2} \text{, which has a minimum value of } 4\Gamma/g_{d} = 2/3. \text{ Scaling of the apparent contact area reduces measured surface (van der Waals) forces (Fig. 15) [8]. However, for aggressively scaled contacts (~50x50nm²), Γ is set by metal-to-metal bonding at the contact asperities (radius~50nm for W with RON=100kΩ [8]), with the associated energy typically in the 0.2µJ/bond range [17].

Using the calibrated analytical relay model with scaled device dimensions, the energy performance (Fig. 16) of 65nm-node relays [1,2] is compared against that of MOSFETs. For A_D = 50x50nm² and the extracted area-dependent portion of Γ (4µJ/µm²), the minimum energy of the relay would be set by the number of bonds. For example, with 5 contact bonds, E_{min} ≈ 4µJ (>10x lower than CMOS) would be achievable.

Conclusion

A pathway to enable reliable micro-relays for digital logic applications through proper contact design is proposed and demonstrated with TiO₂-coated W contacting electrodes. The static and dynamic behavior of these relays is well modeled by the lumped parameter model. Scaled relays appear promising for ultra-low-power applications requiring performance up to ~100MHz.
**Fig. 1:** A schematic 3D view of the electrostatically-actuated relay structure.

**Table I.** Relay device parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Actuation Area, A</td>
<td>$15 \times 30 \mu m^2$</td>
</tr>
<tr>
<td>h</td>
<td>$1 \mu m$</td>
</tr>
<tr>
<td>W</td>
<td>$5 \mu m$</td>
</tr>
<tr>
<td>L</td>
<td>${10, \ldots, 50} \times \mu m$</td>
</tr>
<tr>
<td>g</td>
<td>$200 nm$</td>
</tr>
<tr>
<td>$g_d$</td>
<td>$100 nm$</td>
</tr>
<tr>
<td>Dimple Area, $A_D$</td>
<td>$2 \times {4, 10, 15, 25} \times \mu m^2$</td>
</tr>
</tbody>
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**Fig. 2:** ANSYS simulated displacement contours and the schematic cross-sectional view of the source electrode in the (a) Off state and (b) On state.

**Fig. 3:** 4-mask process flow used to fabricate prototype micro-relays (A-A’ cross-section).

**Fig. 4:** Plan view scanning electron micrograph of a relay before the release step.

**Fig. 5:** (a) Measured $I_D-V_{GS}$ and (b) $I_D-V_{DS}$ characteristics for a relay with $L = 40 \mu m$. The two drains are externally connected.

**Fig. 6:** Measured relay $V_{PI}$ and $V_{RL}$ vs. $L$. $V_{PI}$ and $V_{RL}$ decreases as $L$ increases, as expected. The measured data is within 10% of ANSYS simulation.

**Fig. 7:** (a) ANSYS-simulated displacement contours of the source electrode in the on-state. (b) the spring exhibits both bending and torsional motions when the actuation pad moves.
Fig. 8: Extracted $k_{eff}$ values match ANSYS simulation and the analytical model. As $L$ decreases, torsional motion dominates.

Fig. 9: $V_{RL}^2$ vs. $V_{PI}^2$ for the relays of Fig. 6. $F_A$ is extracted to be 0.45 µN.

Fig. 10: (a) Measured $V_{PI}$ and $F_A$ vs. $T$ for $L=17\mu m$. (b) ANSYS shows that the folded spring design releases the thermal/residual stress by expansion.

Fig. 11: Measured contact resistance vs. temperature for a $L=40\mu m$ relay.

Fig. 12: (a) Relay delay measurement setup. Measurements were made in N$_2$ ambient (b) the delay time $t_{DELAY}$ can be extracted from the difference between the input and output signals. (c) $VPI = t_{DELAY} - t_{CABLE}$, where $t_{CABLE}$ is the electrical delay of the cable.

Fig. 13: Measured $t_D$ vs. $V_{DD}$ for three different relays. $t_D$ reduces as $V_{DD}$ increases, as expected. The Q value is extracted to be 0.3.

Fig. 14: Measured contact resistance vs. number of on/off hot switching cycles (at $V_{DS}=1V$ to mimic scaled-relay operation).

Fig. 15: Extracted average $F_s$ (with standard deviation indicated) vs. $A_p$. Each data point is obtained by measuring more than 10 relays with different $L$ values (Fig. 9).