Since MRAM cells have unlimited write endurance, they can be used as substitutes for DRAMs or SRAMs. MRAMs in electronic appliances enhance their convenience and energy efficiency because data in MRAMs are nonvolatile and retained even in the power-off state. Therefore, 2 to 16Mb standalone MRAMs have been developed [1-4]. However, in terms of their random-access times, they are not enough fast (25ns) [1] as substitutes for all kinds of stand-alone DRAMs or SRAMs. To attain a standalone MRAM with both a random-access time and a large capacity, we adopt a cell structure with 2 transistors and 1 magnetic tunneling junction (2T1MTJ), which we previously published for a 1Mb embedded MRAM macro [5]. We need to develop circuit schemes to achieve a larger memory capacity and a higher cell-occupation ratio with small access-time degradation. We describe the circuit schemes of a 32Mb MRAM, which enable 63% cell occupation ratio and 12ns access time.

Figure 27.4.1 shows a block diagram of 32Mb MRAM. The interface is compatible with asynchronous high-speed SRAMs. Our developed 32Mb MRAM includes four synchronous 10Mb macros (MMAcCs) and peripheral circuits. Each MMAc includes ten 1Mb sub macros (SMaCs). One of the peripheral circuits is an asynchronous-to-synchronous converter and an ECC encoder/decoder using a (32 + 8) bit Reed-Solomon code, which effectively corrects multiple errors. An internal power-supply circuit supplies a 1V core voltage (VDD) and a 1.5V boosted voltage (VBB). Each SMAC includes two redundant columns and two sets of redundant rows.

To achieve an increase of memory capacity, reduction of cell area is essential. The 2T1MTJ cell area is proportional to the writing current for switching the magnetization of the magnetic storage layer. To reduce cell area, we have been reducing the switching current of the magnetic storage layer [6]. As another scheme for cell area reduction, we use boosted a wordline technique in the 32Mb MRAM design. The selected wordline is driven by a voltage VWW, which is higher than VDD. A 1.5V VDD improves drivability of cell transistors, and the gate width of cell transistors is reduced by half, as shown in Fig. 27.4.2. We achieve a memory cell area of 0.66×0.26µm² with a 1mA conducting current. The area is comparable to that of a 6T SRAM in the same process technology.

However, the use of a boosted wordline technique causes access-time degradation because boosted wordline drivers are complicated compared to normal ones. To diminish the degradation, we use a specific type of the wordline driver with an additional power supply, as shown in Fig. 27.4.3. Stand-alone memories are permitted to use an additional power supply because internal power-supply circuits are shared by many memory cell arrays. Since the voltage of a wordline, VWW, is higher than VDD, the wordline driver requires a level converter. In standby mode, the row precharge signal (RP) is at the low level and node one, N1, is precharged to the VWW. Address signals are determined, RP is at VDD and N1 is floating. All decoded signals (X01e~X89A) are at the high level in the selected row, and the selected wordline is driven by VWW. In the boosted driver type, the decoded common line, RXi, connected to the row drivers is driven dynamically. This causes considerable delay due to the parasitic capacitance of large drivers. In contrast, the converter type wordline driver is directly connected to the VDD power line, and the delay in the wordline is reduced.

We design the 1Mb sub-macro using the array architecture shown in Fig. 27.4.4. It is divided by a row decoder, and each 0.5Mb array is composed of eight 64Kb sub arrays. Each sub-array shares write bitlines (WBLi, /WBLi), which are biased in complementary fashion depending on write data to control the switching-current direction in writing. The write circuit is located at the bottom of the memory array. This cell array has long 1.5mm write bitlines for improving the cell occupation ratio. However, the conducting current through the memory cell decreases at a location far from the write driver because of the resistance of the write bitlines. To reduce parasitic resistance of the sink side, our previously published local-current-sink circuits are arranged between each sub-array. The current-sink circuits suppress the decrease of the conducting current, but the suppression is not sufficient when a boosted wordline technique is used.

Since the boosted word line technique improves the driving ability of cell transistors, the bitline voltage of the current-source side, which is at a high level, becomes important. If the bitline voltage of the current-source side is not sufficient for the cell transistors to operate in the saturation region, the driving ability of the cell transistor decreases. Therefore, a technique for reducing the resistance of the current-source side is needed. We develop a spontaneous-write-current assistant (SWCA), which is located at the top of the memory array far from the write drivers. In write mode, the write-enable (WE) signal and the selected write bitline connected to the PMOS (P1) are at the high level, and P1 provides VDD to the write bitline. The SWCAs require only a control signal and substantially reduce the parasitic bitline resistance of the current-source side. We achieve a writing current over 1mA conducting into cells at each of the 2048 rows, and the overhead of the current sink and source circuit areas is about 3% of the memory array area. As a result, 63% cell occupation ratio is achieved. It is estimated at 51% when parity-bit cells for ECC are included as peripheral circuits.

Figure 27.4.5 shows our 2T1MTJ cell and switching-current distributions measured in test elements. We use read-bitline-divided and half-pitch-shift architectures to reduce the access-time. The 2T1MTJ structure is suitable for reducing switching current [6]. The largest switching current is less than 1mA and the mean switching current is 0.6mA.

The simulation results of the 32Mb MRAM in write operation are shown in Fig. 27.4.6, operating in a 12ns cycle. A 12ns read cycle is obtained when the MR ratio is 40%. Power consumption at a 66MHz frequency is estimated at 91mW in write mode and 68mW in read mode. Figure 27.4.7 shows a micrograph of the 32-32 32Mb MRAM using 90nm CMOS. The results in this paper show that 2T1MTJ cell structure is effective for accelerating access time and also increasing memory capacity. Since 2T1MTJ cell area is in proportion to MTJ switching current, we are reducing the switching current using a new type of MTJ [7].

References:
Figure 27.4.1: Block diagram of 32Mb MRAM.

Figure 27.4.2: 2T1MTJ cell area reduction using boosted wordline technique.

Figure 27.4.3: Comparison of wordline driver schemes.

Figure 27.4.4: Write current path in memory cell array.

Figure 27.4.5: 2T1MTJ cell technologies and measured histogram of switching current.

Figure 27.4.6: Simulation results of write mode.
Figure 27.4.7: Micrograph of 32Mb MRAM chip taken after the fourth Cu metal process.

MMAC: 10-Mb macro (8Mb+2Mb)
SMAC: sub macro (1Mb)
PERI: peripheral circuit