EE115C – Spring 2013
Digital Electronic Circuits

Mon & Wed 8:00-9:50am
BH 5249
Topics Covered: Introduction to Digital ICs

- Current equations and parasitic effects of MOS devices
- Technology and layout of digital circuits
- The CMOS inverter
  - Static operation (VTC, noise margins)
  - Propagation delay, power
- Combinational logic and advanced circuit styles
  - Design and sizing (W/L) of logic gates
  - Static, dynamic behavior, and power
- Interconnect: R, and C
- Arithmetic blocks (data paths)
- Sequential logic (latches, flip-flops)
- Timing analysis
Design Abstraction Levels
Course Objectives

❖ Understand, design, and optimize digital circuits with respect to different quality metrics:
  – Power dissipation
  – Speed

❖ Prerequisites:
  – EE115A (analog circuits)
  – M16 (logic design)
Publisher:
Prentice Hall 2003
EE115C Instructors

**Instructor**

Sina Basir-Kazeruni

**Office hours:** 53-145 Eng-IV (5th Floor Lounge)
Mon 12:00 – 1:00pm
Thu 8:00 – 10:00am

**TA**

Abishek Manian

**Office hours:** 67-112 Eng-IV (TA Room)
Wed 12:00 - 1:00pm
Fri 12:00 - 1:00pm
### EE115C Weekly Schedule

<table>
<thead>
<tr>
<th>Day</th>
<th>Time</th>
<th>Mon</th>
<th>Tue</th>
<th>Wed</th>
<th>Thu</th>
<th>Fri</th>
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<td>8</td>
<td>LEC BH 5249</td>
<td>DISC* 5233</td>
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<td>6</td>
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</tbody>
</table>

* Discussion sessions cover identical material
Online Resources

Three places to bookmark:

1. EEWeb
   Grades

2. Piazza
   Q&A

3. Wiki
   Course material
Grades on EEWeb

Any information regarding the course and its instructor can be found on this site. Information regarding instructor e-mail addresses, teaching assistant(s), time schedules, grading, and course material can also be found in the Course Info link.

Course Instructor

Sudhakar Pamarti received the M.S. and the Ph.D. degrees in electrical engineering from the University of California at San Diego in 1999 and 2003, respectively. Since 2005 he has been an assistant professor of electrical engineering at the University of California, Los Angeles. Prior to joining UCLA, he worked with Rambus Inc. developing high speed chip-to-chip electrical communication interfaces.

Teaching Assistant(s)

Abishek Manian
Q&A on Piazza

https://piazza.com/class#spring2013/ee115c
Submission of assignments

Personal queries
  – Before you email, think of WHY can’t you post the question on Piazza
EE115C Digital Electronic Circuits

Contents [hide]
1 Winter 2013 Schedule
2 About EE115C Classwiki
3 Course Feedback: What Do You Think?

This course focuses on introductory-level digital IC design. The topics include:
- Transistor operation in deep-submicron,
- In-depth discussion of the current equations and parasitic capacitances of CMOS transistors
- Study of CMOS inverter and logic gates, including
gate delay calculations,
power consumption,
transistor sizing,
placement for speed/power improvement using both analytical as well as simulation (spice) based studies.
- Dynamic logic gates,
- Sequential circuits,
- Adder architectures.

Course grades are available through EEweb course interface.

Create account
Create a wiki account using your UCLA username

(EE/SEAS/BOL)
24-hour Account Activation

#1: create account

#2: email us your Username

#3: WAIT 24 hours

#4: access local pages
Course Material

- Lecture notes
- Homeworks
- CAD tutorials
- Class project
## Schedule and Syllabus

### Weeks 1-5: Modeling

<table>
<thead>
<tr>
<th>Week</th>
<th>Topic</th>
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<tbody>
<tr>
<td>1</td>
<td>Intro, Scaling</td>
</tr>
<tr>
<td></td>
<td>MOS IV Model</td>
</tr>
<tr>
<td>2</td>
<td>MOS RC Model</td>
</tr>
<tr>
<td></td>
<td>CMOS Inverter VTC</td>
</tr>
<tr>
<td>3</td>
<td>Delay Analysis</td>
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<tr>
<td></td>
<td>Power Consumption</td>
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<tr>
<td>4</td>
<td>CMOS Logic</td>
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<tr>
<td></td>
<td>Gate Sizing</td>
</tr>
<tr>
<td>5</td>
<td>Logical Effort</td>
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<tr>
<td></td>
<td>Wires, Elmore Delay</td>
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### Weeks 6-10: Design

<table>
<thead>
<tr>
<th>Week</th>
<th>Topic</th>
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<tbody>
<tr>
<td>6</td>
<td>Midterm</td>
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<tr>
<td></td>
<td>Stick Diagrams, Adder Blocks</td>
</tr>
<tr>
<td>7</td>
<td>Adders, Layout Design Rules</td>
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<tr>
<td></td>
<td>Pass-Transistor Logic</td>
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<tr>
<td>8</td>
<td>Basic Tree Adders</td>
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<td>Latches and Flip-Flop</td>
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<td>No Class</td>
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<td></td>
<td>Setup and Hold Times</td>
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<tr>
<td>10</td>
<td>Timing Analysis</td>
</tr>
<tr>
<td></td>
<td>Perspectives / Review</td>
</tr>
</tbody>
</table>
Grading Policy & Organization

14%  7 homeworks
25%  Project
25%  Midterm
35%  Final
1%   Survey
## Gantt Chart

**Week** | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11
---|---|---|---|---|---|---|---|---|---|---|---
Hw #1 | | | | | | | | | | | |
Hw #2 | | | | | | | | | | | |
Hw #3 | | | | | | | | | | | |
Hw #4 | | | | | | | | | | | |
Hw #5 | | | | | | | | | | | |
Hw #6 | | | | | | | | | | | |
Hw #7 | | | | | | | | | | | |
Project | | | | | | | | | | | |
Midterm | | | | | | | | | | | |
Final Exam | | | | | | | | | | | |

**EE115C – Spring 2013**
Exams: Closed Book

- **Midterm:** Mon May 06, 8:00-9:50am
  - 1 page of notes

- **Final:** Mon Jun 10, 6:30pm-9:30pm
  - 1 sheet (2 pages) of notes
Lab Sessions

- **Week 2:** regular discussion
- **Weeks 8 & 9:** extra sessions (project help)
Software

- **Cadence software**
  - Online documentation and tutorials

- **90nm CMOS technology (Cadence GPDK)**
  - 9 metal layers

- **Important tools / skills**
  - Design Capture: Virtuoso Schematic / Layout Editor
  - Circuit Simulation: Spectre / Ocean
  - Design Verification (DRC, LVS, Extraction): Assura/QRC

*Updated tutorials (Cadence 6) available on the wiki*

*Old page: http://www.ee.ucla.edu/~dejan/ee115c*
EE115C Design Flow

- Schematic symbols & CDFs
  - Virtuoso
- Layouts & pcells
  - Vitruoso, VXL
- Verification
  - DRC & LVS, RCX
- Simulation
  - Analog Env. Spectre
- Compare results (finish)
- Assura database
- Spectre models

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Anatomy of the Flow: 
Cadence PDK Database

- Schematic symbols & CDFs
  - Virtuoso

- Layout & pcells
  - Vitruoso
  - VXL

- Assura database
  - DRC & LVS
  - RCX

- Verification
  - Analog Env.
  - Spectre

- Simulation
  - Analog Env.
  - Spectre

- Compare results (finish)

- Spectre models
Anatomy of the Flow: Virtuoso Schematic and Layout Editor

- **Schematic**
  - Symbols & CDFs
  - Virtuoso

- **Layout**
  - Layouts & pcells
  - Vitruoso, VXL

- **Verification**
  - Assura database
  - DRC & LVS, RCX

- **Simulation**
  - Analog Env. Spectre

- **Compare Results (finish)**

- **Spectre Models**
Anatomy of the Flow: Assura Design Verification

- Schematic symbols & CDFs
- Layouts & pcells
- Assura database

Schematic: Virtuoso

Layout: Virtuoso, VXL

Verification: DRC & LVS, RCX

Simulation: Analog Env. Spectre

Compare results (finish)

Spectre models
Anatomy of the Flow: Spectre Simulation Environment

- schematic symbols & CDFs
  - schematic
    - Virtuoso
  - layout
    - Vitruoso
    - VXL
  - verification
    - DRC & LVS
    - RCX

- comparison
  - Analog Env.
    - Spectre

- compare results
  - Analog Env.
    - Spectre

- Spectre models
Flow Walkthrough: Enter the Flow

- schematic symbols & CDFs
- layouts & pcells
- Assura database
- schematic
  - Virtuoso
- layout
  - Virtuoso
  - VXL
- verification
  - DRC & LVS
  - RCX
- simulation
  - Analog Env. Spectre
- compare results (finish)
- simulation
  - Analog Env. Spectre
- Spectre models
Flow Walkthrough:
#1: Schematic Capture

- schematic symbols & CDFs → schematic
- layout → layout
- verification → DRC & LVS
- Assura database

- schematic in Virtuoso
- layouts & pcells in Vitruoso & VXL
- Assura database in RCX

Simulation in Spectre
- Analog Env.
- Compare results (finish)
Flow Walkthrough: #2: Circuit Simulation

1. schematic symbols & CDFs → schematic
2. simulation → Analog Env. Spectre
3. layouts & pcells → schematic
4. Assura database
Flow Walkthrough:
#3: Layout Capture

1. schematic
   - Virtuoso

2. schematic
   - simulation

3. layout
   - Vitruoso
   - VXL

4. verification
   - DRC & LVS
   - RCX

Assura database

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Flow Walkthrough: #4: Design Verification

1. Schematic symbols & CDFs
2. Schematic
   - Virtuoso
3. Layouts & pcells
   - Vitruoso
   - VXL
4. Verification
   - DRC & LVS
   - RCX
5. Assura database

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Flow Walkthrough: #5: Post-Layout Simulation

1. schematic
   - Virtuoso

2. schematic simulation results

3. layout
   - Virtuoso
   - VXL

4. verification
   - DRC & LVS
   - RCX

5. simulation
   - Analog Env.
   - Spectre

6. compare results (finish)

Input:
- schematic symbols & CDFs
- layouts & pcells
- Assura database

Output:
- schematic simulation results
- compare results (finish)
Flow Walkthrough: #6: Comparison of Results

1. schematic
   - Virtuoso

2. schematic simulation results

3. layout
   - Virtuoso
   - VXL

4. verification
   - DRC & LVS
   - RCX

5. post-layout simulation results

6. compare results (finish)
## Online Tutorials:
Start from Here (Use Design-Flow Path Later)

<table>
<thead>
<tr>
<th>Tutorial #</th>
<th>Content</th>
<th>Learning</th>
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<tbody>
<tr>
<td>Tutorial 1</td>
<td>Account and Tool Setup</td>
<td>Account and Cadence library setup, transistor IV curves.</td>
</tr>
<tr>
<td>Tutorial 2</td>
<td>Hierarchical Schematic and Simulation</td>
<td>Technology calibration (Ring OSC, FO4), Spectre simulator.</td>
</tr>
<tr>
<td>Tutorial 3</td>
<td>Virtuoso Layout Editing (DRC, LVS)</td>
<td>Layout rules (DRC, LVS), custom standard cell (INVX1).</td>
</tr>
<tr>
<td>Tutorial 4</td>
<td>Schematic-driven Layout (Virtuoso XL)</td>
<td>Advanced layout, standard-cell design (NAND2X1).</td>
</tr>
<tr>
<td>Tutorial 5</td>
<td>Hierarchical Design and Post-Layout Verification</td>
<td>Hierarchical design, post-layout verification.</td>
</tr>
<tr>
<td>Tutorial 6</td>
<td>Advanced simulation using OCEAN environment</td>
<td>Automating simulations and data measurement.</td>
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</table>
Assignment 1: Getting Cadence to Work

- After setting up Cadence (classwiki / Tool setup):
  - Complete Tutorial 1.1 posted on classwiki.
  - Turn in a screenshot (email ee115c.s13@gmail.com)

We are looking for this

![Image of Library Manager]

and this

```
Log file is "/w/class.1/ee/ee115v/ee115vta/ee115c_sina/libManager.log".
Created new library "ee115c" at /w/class.1/ee/ee115v/ee115vta/ee115c_sina/ee115c.
```
Lecture 1:
Introduction
Look Familiar?
A Look Under the Hood…

Cell Processor

- Computer that acts like cells in a biological system
- High-performance distributed computing
- 10x faster than other CPUs

IBM, Sony, Toshiba

Let’s look back to see how it all started…
A Bit of History... The First Computer (1832)

- The Babbage Difference Engine
  - 25,000 parts
  - cost: £17,470
The First Digital Electronic Computer

Zuse Z3
(1941)

Device: Electromechanical relay

Binary
5 – 10 Hz
22b words

2K relays
Five Years Later

ENIAC
(1946)

Device: Vacuum tube

Decimal
5M joints
hand-soldered

18K
tubes

150kW

$500K

$6M today

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The First PC

Simon (1950)

Device: Electromechanical relay

4 ops: +, −x, >, S
2b Reg/ALU

$600
What is the Machine’s Future?

Mr. Berkeley's answer:

"Simon has two futures. In first place Simon can grow. With another chassis and some wiring and engineering, the machine will be able to compute decimally. Perhaps in six months more, we may be able to have it working on real problems. In the second place, Simon may start a fad of building baby mechanical brains, similar to the hobby of building crystal radio sets that swept the country in the 1920's."

[1956 Berkeley Enterprises Report]
Squee (The Electronic Robot Squirrel)

[1956 Berkeley Enterprises Report]
The Transistor Revolution (1948)

First transistor
Bell Labs (1948)
The First Integrated Circuit (1958)

7/16" wide and containing two transistors, mounted on a bar of germanium
(Image courtesy of Texas Instruments, Inc.)
The First Integrated Circuits (1960’s)

Bipolar logic (1960’s)

ECL 3-input Gate
Motorola (1966)
Integrated Electronics

1948 (Bell Labs)

1958 (TI)

1971 (Intel)

BJT

IC

μP

4004

108kHz
Intel 4004 Microprocessor (1971)

2,300 transistors (12mm²)
108 KHz operation (10μm)
“Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate.” Electronics, Volume 38, Number 8, April 19, 1965
Moore’s Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months

“The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term, this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.”

[G. Moore, Electronics, 1965]
Transistors / cm²

40 years

2,000,000x improvement

Courtesy: Broadcom

<table>
<thead>
<tr>
<th>Year</th>
<th>Size (μm)</th>
<th>Transistors</th>
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<tbody>
<tr>
<td>1972</td>
<td>10</td>
<td>2K</td>
</tr>
<tr>
<td>1982</td>
<td>5</td>
<td>50K</td>
</tr>
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<td>1992</td>
<td>1</td>
<td>2M</td>
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<td>2002</td>
<td>130</td>
<td>100M</td>
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<tr>
<td>2012</td>
<td>20</td>
<td>4B</td>
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Scaling

Voltage: $V_{DD}, V_T$
Size: $W, L, t_{ox}$
Dennard’s Classical MOSFET Scaling (1974)

<table>
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<th>Scaling Factor</th>
<th>Device or Circuit Parameter</th>
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<tbody>
<tr>
<td>1/κ</td>
<td>Device dimension $t_{ox}$, L, W</td>
</tr>
<tr>
<td>κ</td>
<td>Doping concentration $N_a$</td>
</tr>
<tr>
<td>1/κ</td>
<td>Voltage $V$</td>
</tr>
<tr>
<td>1/κ</td>
<td>Current $I$</td>
</tr>
<tr>
<td>1/κ</td>
<td>Capacitance $\varepsilon A/t_{ox}$</td>
</tr>
<tr>
<td>1/κ²</td>
<td>Delay time/circuit $V_C/I$</td>
</tr>
<tr>
<td>1/κ²</td>
<td>Power dissipation/circuit $V_I$</td>
</tr>
<tr>
<td>1</td>
<td>Power density $V_I/A$</td>
</tr>
</tbody>
</table>

Constant E-field Scaling

Voltage and size scale by the same factor, S (S > 1)
- \( E = \frac{V}{L} = \text{constant} \)

Outcomes:
- More transistors/area \( \frac{1}{S^2} \)
- Faster delay \( \frac{1}{S} \)
- Lower energy/op \( \frac{1}{S^3} \)

Problem: \( V_T \) scaling (exponential leakage)
Constant E-field Scaling

Ended at the 130nm node
Historical Scaling Trends

- **Power density**
- **Leakage power**

![Graph showing historical scaling trends with frequency on the y-axis and year on the x-axis. Key points include 1970, 1980, 1990, 2000, 2010.](Image)

- **Generation**
  - BJT
  - nMOS
  - CMOS

- **Components**
  - 8008, 8080, 8085, 8086, 286, 386

- **Processes**
  - Pentium
  - Pentium Pro
  - Pentium 4

- **Comments**
  - Courtesy: S. Borkar (Intel)

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Technology Scaling is Power Driven

CMOS delivered better cost performance
- It was more energy efficient
- It improved the integration level
Bipolar → Power Wall → CMOS

- **Technologies:** bipolar, nMOS, CMOS
- **Constant voltage scaling:** increasing power

![Diagram showing the evolution of module heat flux with time, highlighting the transition from bipolar to CMOS technologies.](image)

*Courtesy: Roger Schmidt (IBM)*
## Scaling Scenarios: Fixed V, Fixed E, General

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Relation</th>
<th>Fixed V</th>
<th>Fixed E</th>
<th>General</th>
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<tbody>
<tr>
<td>( W, L, t_{ox} )</td>
<td>1/S</td>
<td>1/S</td>
<td>1/S</td>
<td>1/S</td>
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<tr>
<td>( V_{DD}, V_T )</td>
<td>1</td>
<td>1/S</td>
<td>1/U</td>
<td>1/U</td>
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<tr>
<td>Area/Device</td>
<td>WL</td>
<td>1/S²</td>
<td>1/S²</td>
<td>1/S²</td>
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<tr>
<td>( C_{ox} )</td>
<td>1/t_{ox}</td>
<td>S</td>
<td>S</td>
<td>S</td>
</tr>
<tr>
<td>( C_{gate} )</td>
<td>( C_{ox} ) WL</td>
<td>1/S</td>
<td>1/S</td>
<td>1/S</td>
</tr>
<tr>
<td>( k_n, k_p )</td>
<td>( C_{ox} ) W/L</td>
<td>S</td>
<td>S</td>
<td>S</td>
</tr>
<tr>
<td>( I_{sat} )</td>
<td>( C_{ox} ) WV</td>
<td>1</td>
<td>1/S</td>
<td>1/U</td>
</tr>
<tr>
<td>Current Density</td>
<td>( I_{sat} / \text{Area} )</td>
<td>S²</td>
<td>S</td>
<td>S²/U</td>
</tr>
<tr>
<td>( R_{on} )</td>
<td>( V / I_{sat} )</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Intr. Delay</td>
<td>( R_{on} ) ( C_{gate} )</td>
<td>1/S</td>
<td>1/S</td>
<td>1/S</td>
</tr>
<tr>
<td>Power</td>
<td>( I_{sat} ) ( V )</td>
<td>1</td>
<td>1/S²</td>
<td>1/U²</td>
</tr>
<tr>
<td>P Density</td>
<td>Power/Area</td>
<td>S²</td>
<td>1</td>
<td>S²/U²</td>
</tr>
</tbody>
</table>
General Scaling

Size scaling $S >$ Voltage scaling $U$

Voltage scaling slowing down
- $V_T$ determined by leakage
- $t_{ox}$ also set by leakage

Current increasing by stressing silicon
CMOS Scaling is Continuing to Change

- **1990’s**: both $V_{DD}$ and $L$ scaling
- **2000’s**: $V_{DD}$ scaling slowing down, $L$ scaling
- **2010’s**: rate of $L$ scaling slowing down

Energy efficiency = \[ \frac{1}{C_{sw} \cdot V_{DD}^2 \cdot (1+E_{lk}/E_{sw})} \]

Energy Efficiency (GOPS/mW) vs. Technology Generation (nm)
More than Moore: 2010+

[ITRS 2010]
Approaching Atomic Limits

Si atom
0.25nm

20nm FET

80x

1x

Hair
50,000 nm

200,000x
Technology: alternative structures and materials, post-silicon devices

Design: billion transistors, GHz operation

Source: K. Cao (ASU)
Replacing CMOS by another more energy efficient technology is a distant prospect now

Low-power high-speed CMOS technology is becoming an indispensable, rather than desirable, technology

Power is the main challenge we need to address