EE115C – Winter 2017
Digital Electronic Circuits

Tue & Thu 4:00-5:50pm
2760 Boelter Hall
Topics Covered: Introduction to Digital ICs

- Current equations and parasitic effects of MOS devices
- Technology and layout of digital circuits
- The CMOS inverter
  - Static operation (VTC, noise margins)
  - Propagation delay, power
- Combinational logic and advanced circuit styles
  - Design and sizing (W/L) of logic gates
  - Static, dynamic behavior, and power
- Interconnect: R, and C
- Arithmetic blocks (data paths)
- Sequential logic (latches, flip-flops)
- Timing analysis
Design Abstraction Levels
Course Objectives

- Understand, design, and optimize digital circuits with respect to different quality metrics:
  - Power dissipation
  - Speed

- Prerequisites:
  - EE115A (analog circuits)
  - M16 (logic design)
Publisher:
Prentice Hall 2003
EE115C Instructors

Prof. Dejan Marković

Office hours
- Tue 10:30am-12pm
- Fri 9:30-11am
- 56-147E Eng-IV Bldg

Mahmoud Elhebeary

Office hours
- Thu 1-2pm
- Fri 4-5pm
- CAD tools, labs, project
# EE115C Weekly Schedule

<table>
<thead>
<tr>
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<tbody>
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<tr>
<td>Tue</td>
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<td></td>
<td></td>
<td></td>
<td>Lecture 2760 Boelter</td>
</tr>
<tr>
<td>Wed</td>
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<td>Fri</td>
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</tbody>
</table>

* Discussion sessions cover identical material
Online Resources

Three places to bookmark:

1. Wiki
   - Course material

2. Piazza
   - Q&A

3. MyUCLA
   - Grades
EE115C Digital Electronic Circuits

Course Description
This course focuses on introductory-level digital IC design. The topics include:
- Transistor operation in deep-submicron,
- In-depth discussion of the current equations and parasitic capacitances of CMOS transistors
- Study of CMOS inverter and logic gates, including
gate delay calculations,
power consumption,
transistor sizing,
placement for speed/power improvement using both analytical as well as simulation (spice) based studies.
- Dynamic logic gates,
Sequential circuits,
Adder architectures.

Course grades are available through MyUCLA.

Winter 2017
Lectures
- Tue & Thu, 4:00-5:50pm, 2760 Boelter Hall (map: Interactive)

Discussions
- Dis. 1A: Fri 2:00-2:50pm, 2258A Franz Hall
- Dis. 1B: Thu 10:00-10:50am, A51 Humanities

Has links to Piazza and MyUCLA
Submission of assignments

Personal queries
Course Material

- Lecture notes
- Homeworks
- CAD tutorials
- Class project
# Schedule and Syllabus

## Weeks 1-5: Modeling

<table>
<thead>
<tr>
<th>Week</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Intro, Scaling</td>
</tr>
<tr>
<td></td>
<td>MOS IV Model</td>
</tr>
<tr>
<td>2</td>
<td>MOS RC Model</td>
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<tr>
<td></td>
<td>CMOS Inverter VTC</td>
</tr>
<tr>
<td>3</td>
<td>Delay Analysis</td>
</tr>
<tr>
<td></td>
<td>Power Consumption</td>
</tr>
<tr>
<td>4</td>
<td>CMOS Logic</td>
</tr>
<tr>
<td></td>
<td>Gate Sizing</td>
</tr>
<tr>
<td>5</td>
<td>Logical Effort Theory</td>
</tr>
<tr>
<td></td>
<td>Midterm</td>
</tr>
</tbody>
</table>

## Weeks 6-10: Design

<table>
<thead>
<tr>
<th>Week</th>
<th>Topic</th>
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<tbody>
<tr>
<td>6</td>
<td>Wires, Elmore Delay</td>
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<tr>
<td></td>
<td>Layout: Stick Diagrams</td>
</tr>
<tr>
<td>7</td>
<td>Adder Building Blocks</td>
</tr>
<tr>
<td></td>
<td>Pass-Transistor Logic</td>
</tr>
<tr>
<td>8</td>
<td>Basic Tree Adders</td>
</tr>
<tr>
<td></td>
<td>Latches and Flip-Flops</td>
</tr>
<tr>
<td>9</td>
<td>Setup and Hold Times</td>
</tr>
<tr>
<td></td>
<td>Timing Analysis</td>
</tr>
<tr>
<td>10</td>
<td>Project Presentations</td>
</tr>
<tr>
<td></td>
<td>Review for Final Exam</td>
</tr>
</tbody>
</table>
Grading Policy & Organization

- 15% Homework (7)
- 25% Project
- 25% Midterm
- 35% Final
Exams: Closed Book

- **Midterm:** Thu Feb 9, 4:00-5:50pm
  - 1 page of notes

- **Final:** Wed Mar 22, 11:30am-2:30pm
  - 1 sheet (2 pages) of notes
Lab Sessions

- **Weeks 8 & 9:** extra sessions (project help)

![Schedule diagram]

- **Project**
  - **Start:** Week 8
  - **Due:** Week 9

- **Extra Labs**

<table>
<thead>
<tr>
<th>Week</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
</table>

Software

- **Cadence software**
  - Online documentation and tutorials

- **90nm CMOS technology (Cadence GPDK)**
  - 9 metal layers

- **Important tools / skills**
  - Design Capture: Virtuoso Schematic / Layout Editor
  - Circuit Simulation: Spectre / Ocean
  - Design Verification (DRC, LVS, Extraction): Assura/QRC

*Cadence tutorials are on the wiki*
Anatomy of the Flow: Cadence PDK Database

- **Schematic**: Symbols & CDFs (Virtuoso)
- **Layout**: Layouts & pCells (Vitruoso, VXL)
- **Verification**: Assura database (DRC & LVS, RCX)
- **Simulation**: Analog Env. Spectre
- **Compare Results**: (finish)
- **Spectre Models**
Anatomy of the Flow: Virtuoso Schematic and Layout Editor
Anatomy of the Flow: Assura Design Verification

- schematic symbols & CDFs
- layouts & pcells
- Assura database
- schematic: Virtuoso
- layout: Virtuoso, VXL
- verification: DRC & LVS, RCX
- simulation: Analog Env. Spectre
- compare results (finish)
- simulation: Analog Env. Spectre
- Spectre models
Anatomy of the Flow: Spectre Simulation Environment

- schematic symbols & CDFs
- layouts & pcells
- Assura database
- schematic
  - Virtuoso
- layout
  - Virtuoso
  - VXL
- verification
  - DRC & LVS
  - RCX
- simulation
  - Analog Env. Spectre
- compare results (finish)
- simulation
  - Analog Env. Spectre
- Spectre models
Flow Walkthrough: Enter the Flow

1. Schematic
   - schematic symbols & CDFs
   - Virtuoso

2. Layout
   - layout & pcells
   - Vitruoso
   - VXL

3. Verification
   - verification
   - DRC & LVS
   - RCX

4. Simulation
   - simulation
   - Analog Env.
   - Spectre

5. Compare Results (finish)

6. Spectre models

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Flow Walkthrough:
#1: Schematic Capture

1. **Schematic Capture**
   - **Vitruoso**
   - **Symbols & CDFs**

2. **Layout Capture**
   - **Vitruoso**
   - **VXL**

3. **Verification**
   - **DRC & LVS**
   - **RCX**

4. **Assura Database**

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Flow Walkthrough: #2: Circuit Simulation

1. Schematic
   - layout & pcells
   - symbols & CDFs

2. Simulation
   - Analog Env.
   - Spectre
   - models

3. Compare results
   - finish

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Flow Walkthrough: #3: Layout Capture

1. schematic symbols & CDFs
2. schematic simulation
3. layout
4. verification

schematic symbols & CDFs
layout & pcells
Assura database

Virtuoso
VXL

DRC & LVS
RCX

VDD
GND
Flow Walkthrough: #4: Design Verification

1. schematic
   - Virtuoso

2. layout
   - Vitruoso
   - VXL

3. schematic symbols & CDFs

4. layouts & pcells
   - Vitruoso
   - VXL

5. verification
   - DRC & LVS
   - RCX

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Flow Walkthrough: #5: Post-Layout Simulation

1. Schematic
   - Symbols & CDFs
   - Virtuoso

2. Schematic Simulation Results
   - Compare results (finish)

3. Layout
   - Layouts & pcells
   - Vitruoso
   - VXL

4. Verification
   - DRC & LVS
   - RCX

5. Simulation
   - Analog Env. Spectre

6. Spectre Models

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Flow Walkthrough:
#6: Comparison of Results

1. schematic symbols & CDFs → schematic → Virtuoso
2. schematic simulation results
3. layouts & pcells → layout → Virtuoso, VXL
4. verification → DRC & LVS, RCX
5. post-layout simulation results
6. compare results (finish)
## Things You Will Learn

<table>
<thead>
<tr>
<th>Tutorial #</th>
<th>Content</th>
<th>Learning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tutorial 1</td>
<td>Account and Tool Setup</td>
<td>Account and Cadence library setup, transistor IV curves.</td>
</tr>
<tr>
<td>Tutorial 2</td>
<td>Hierarchical Schematic and Simulation</td>
<td>Technology calibration (Ring OSC, FO4), Spectre simulator.</td>
</tr>
<tr>
<td>Tutorial 3</td>
<td>Virtuoso Layout Editing (DRC, LVS)</td>
<td>Layout rules (DRC, LVS), custom standard cell (INVX1).</td>
</tr>
<tr>
<td>Tutorial 4</td>
<td>Schematic-driven Layout (Virtuoso XL)</td>
<td>Advanced layout, standard-cell design (NAND2X1).</td>
</tr>
<tr>
<td>Tutorial 5</td>
<td>Hierarchical Design and Post-Layout Verification</td>
<td>Hierarchical design, post-layout verification.</td>
</tr>
<tr>
<td>Tutorial 6</td>
<td>Advanced simulation using OCEAN environment</td>
<td>Automating simulations and data measurement.</td>
</tr>
</tbody>
</table>
Assignment 1: Getting Cadence to Work

- After setting up Cadence (classwiki / Tool setup):
  - Complete Tutorial 1.1 posted on classwiki.
  - Turn in a screenshot (email ee115c.w17@gmail.com)

We are looking for this

and this

Log file is "/w/class.1/ee/ee115v/ee115vta/ee115c_sina/libManager.log".
Created new library "ee115c" at /w/class.1/ee/ee115v/ee115vta/ee115c_sina/ee115c.
Lecture 1:
Introduction
A Bit of History... The First Computer (1832)

- The Babbage Difference Engine
  - 25,000 parts
  - cost: £17,470
The First Digital Electronic Computer

Zuse Z3
(1941)

Device: Electromechanical relay

Binary
5 – 10 Hz
22b words

2K relays
Five Years Later

**ENIAC**
(1946)

- **Device:** Vacuum tube
- **18K tubes**
- **150kW**
- **$500K**
- **$6M today**

**Decimal**

- **5M joints**
- hand-soldered

Google images
The First PC

Simon (1950)

Device: Electromechanical relay

4 ops: +, −x, >, S
2b Reg/ALU

$600
What is the Machine’s Future?

Mr. Berkeley's answer:

"Simon has two futures. In first place Simon can grow. With another chassis and some wiring and engineering, the machine will be able to compute decimally. Perhaps in six months more, we may be able to have it working on real problems. In the second place, Simon may start a fad of building baby mechanical brains, similar to the hobby of building crystal radio sets that swept the country in the 1920's."

[1956 Berkeley Enterprises Report]
Squee (The Electronic Robot Squirrel)

[1956 Berkeley Enterprises Report]
The Transistor Revolution (1948)

First transistor
Bell Labs (1948)
The First Integrated Circuit (1958)

7/16" wide and containing two transistors, mounted on a bar of germanium
(Image courtesy of Texas Instruments, Inc.)
The First Integrated Circuits (1960’s)

Bipolar logic (1960’s)

ECL 3-input Gate Motorola (1966)
Integrated Electronics

1948 (Bell Labs) → BJT

1958 (TI) → IC

1971 (Intel) → μP

4004
108kHz

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Intel 4004 Microprocessor (1971)

2,300 transistors (12mm$^2$)
108 KHz operation (10μm)
“Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate.” Electronics, Volume 38, Number 8, April 19, 1965

1965 Data (Moore)
Moore’s Law

In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.

“The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term, this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.”

[G. Moore, Electronics, 1965]
2005
Transistors / cm²

40 years

2,000,000x improvement

Courtesy: Broadcom

<table>
<thead>
<tr>
<th>Year</th>
<th>Width (μm)</th>
<th>Transistors/cm²</th>
</tr>
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<tbody>
<tr>
<td>1972</td>
<td>10</td>
<td>2K</td>
</tr>
<tr>
<td>1982</td>
<td>5</td>
<td>50K</td>
</tr>
<tr>
<td>1992</td>
<td>1</td>
<td>2M</td>
</tr>
<tr>
<td>2002</td>
<td>130nm</td>
<td>100M</td>
</tr>
<tr>
<td>2012</td>
<td>20nm</td>
<td>4B</td>
</tr>
</tbody>
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Scaling

Voltage: \( V_{DD}, V_T \)

Size: \( W, L, t_{ox} \)
### Dennard’s Classical MOSFET Scaling (1974)

**Scaling Factor**  
**Device or Circuit Parameter**

- $1/\kappa$: Device dimension $t_{ox}$, $L$, $W$
- $\kappa$: Doping concentration $Na$
- $1/\kappa$: Voltage $V$
- $1/\kappa$: Current $I$
- $1/\kappa$: Capacitance $\varepsilon A/t_{ox}$
- $1/\kappa^2$: Delay time/circuit $VC/I$
- $1/\kappa^2$: Power dissipation/circuit $VI$
- $1$: Power density $VI/A$

---

Constant E-field Scaling

Voltage and size scale by the same factor, $S$ ($S > 1$)
- $E = \frac{V}{L} = \text{constant}$

Outcomes:
- More transistors/area $\frac{1}{S^2}$
- Faster delay $\frac{1}{S}$
- Lower energy/op $\frac{1}{S^3}$

Problem: $V_T$ scaling (exponential leakage)
Constant E-field Scaling

Ended at the 130nm node
Historical Scaling Trends

![Graph showing historical scaling trends in computing performance from 1970 to 2010. The graph plots frequency (MHz) against year, with key milestones such as the 8008, 8086, 8085, 8080, 4004, 386, 286, Pentium Pro, and Pentium 4 processors highlighted. Key periods marked with 'Const V_{DD}', 'Const E', and 'General'.

Power density and leakage power are also indicated on the graph.}

Courtesy: S. Borkar (Intel)
Technology Scaling is Power Driven

- CMOS delivered better cost performance
  - It was more energy efficient
  - It improved the integration level
Bipolar → Power Wall → CMOS

- **Technologies:** bipolar, nMOS, CMOS
- **Constant voltage scaling:** increasing power

![Graph showing module heat flux over time](image)

*Courtesy: Roger Schmidt (IBM)*
## Scaling Scenarios: Fixed V, Fixed E, General

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Relation</th>
<th>Fixed V</th>
<th>Fixed E</th>
<th>General</th>
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</thead>
<tbody>
<tr>
<td>$W, L, t_{ox}$</td>
<td></td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>$V_{DD}, V_T$</td>
<td>$1$</td>
<td></td>
<td>$1/S$</td>
<td>$1/U$</td>
</tr>
<tr>
<td>Area/Device</td>
<td>WL</td>
<td>$1/S^2$</td>
<td>$1/S^2$</td>
<td>$1/S^2$</td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>$1/t_{ox}$</td>
<td>$S$</td>
<td>$S$</td>
<td>$S$</td>
</tr>
<tr>
<td>$C_{gate}$</td>
<td>$C_{ox} \cdot WL$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>$k_n, k_p$</td>
<td>$C_{ox} \cdot W/L$</td>
<td>$S$</td>
<td>$S$</td>
<td>$S$</td>
</tr>
<tr>
<td>$I_{sat}$</td>
<td>$C_{ox} \cdot WV$</td>
<td>$1$</td>
<td>$1/S$</td>
<td>$1/U$</td>
</tr>
<tr>
<td>Current Density</td>
<td>$I_{sat} / \text{Area}$</td>
<td>$S^2$</td>
<td>$S$</td>
<td>$S^2/U$</td>
</tr>
<tr>
<td>$R_{on}$</td>
<td>$V / I_{sat}$</td>
<td>$1$</td>
<td>$1$</td>
<td>$1$</td>
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<tr>
<td>Intr. Delay</td>
<td>$R_{on} \cdot C_{gate}$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
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<tr>
<td>Power</td>
<td>$I_{sat} \cdot V$</td>
<td>$1$</td>
<td>$1/S^2$</td>
<td>$1/U^2$</td>
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<tr>
<td>P Density</td>
<td>Power/Area</td>
<td>$S^2$</td>
<td>$1$</td>
<td>$S^2/U^2$</td>
</tr>
</tbody>
</table>
General Scaling

Size scaling $S >$ Voltage scaling $U$

Voltage scaling slowing down
- $V_T$ determined by leakage
- $t_{ox}$ also set by leakage

Current increasing by stressing silicon
CMOS Scaling is Continuing to Change

- **1990’s**: both $V_{DD}$ and $L$ scaling
- **2000’s**: $V_{DD}$ scaling slowing down, $L$ scaling
- **2010’s**: rate of $L$ scaling slowing down

Energy efficiency = \( \frac{1}{C_{sw} \cdot V_{DD}^2 \cdot (1+E_{lk}/E_{sw})} \)

![Graph showing energy efficiency vs technology generation](image-url)

- $L$ delayed
- mostly $L$
- $L$ & $V_{DD}$

**Equation**

\[
\text{Energy efficiency} = \frac{1}{C_{sw} \cdot V_{DD}^2 \cdot (1+E_{lk}/E_{sw})}
\]
More than Moore: 2010+

[ITRS 2010]
Approaching Atomic Limits

Si atom 0.25nm

20nm FET

1x

80x

200,000x

Hair 50,000 nm
Scaling Toward 10nm Node

- **Technology**: alternative structures and materials, post-silicon devices
- **Design**: billion transistors, GHz operation

Source: K. Cao (ASU)
CMOS Replacement?

- Replacing CMOS by another more energy efficient technology is a distant prospect now.

- Low-power high-speed CMOS technology is becoming an indispensable, rather than desirable, technology.

- Power is the main challenge we need to address.