EE115C – Digital Electronic Circuits

Tutorial 4:
Schematic-driven Layout (Virtuoso XL)

This tutorial will demonstrate schematic-driven layout on the example of a 2-input NAND gate.

Simple Layout (that won’t work)

Startup Cadence and go to the Library Manager and create new cell NAND2X1 in your ee115c library. Begin with the layout view: you will shortly see the need for Virtuoso XL (VXL). In your NAND2X1 layout, instantiate an NMOS transistor.

Go back to your Virtuoso Layout Editing window and place the instance. The transistor will looks quite small on the screen, so press ‘f’ (zoom to fit). The layout should look like this:
Now, let’s edit instance properties to make a stacked device. Press ‘q’ to edit object properties.

Set **Total Width** to 750n (press tab and **Finger Width** will automatically be changed to 750n).

Since we plan to use this device for a 2-input NAND gate, change fingers to 2.

Click **OK**.

Two nMOS merged (stacked) together should appear. Type ‘f’ (the hot key for Fit All under the Window menu) and the layout should appear centered in the window.
Your screen should now look like this:

**Tip:** you can undo whatever you have just done in Virtuoso. Use the ‘u’ hot key or select **Undo** from the **Edit** menu. You may also redo what you have just undone using the **Shift-u** hotkey.

Now we have a problem! Extra contacts in the source/drain areas cannot be removed in order to create an NMOS stack. The “out-of-box” transistor pcell (parameterizable cell) does not have an option of merging the overlapping source and drain areas in the middle. This design kit was intended for analog / mixed-signal design, so this isn’t totally unexpected! The kit can be made to work well for digital functionality with help from another tool: Virtuoso-XL (VXL). Typically, analog layout is done in a full-custom way, while digital layout is often created with help from tools to handle design complexity.

## Creating Layout using Virtuoso XL (VXL)

Virtuoso XL is a schematic-driven layout generation tool. First, delete the transistor you have and start with an empty layout window of NAND2 cell. Next, create the schematic view of the **NAND2X1** cell. Point inside the **Virtuoso Schematic Editing** window and type ‘i’ to instantiate a transistor:
Choose or type symbol view.

Set Total Width and Finger Width to 480nm.

Click Hide to add an instance to your schematic.

This is a four-terminal NMOS device. Place two transistors in the Virtuoso Schematic Editor to form NMOS stack for a NAND2X1 gate. You also need to add the PMOS devices for your NAND gate (two PMOS devices in parallel with width of 480nm each to form your pull-up network).

Also add input/output pins to your schematic: to do that, hot ‘p’ in the editor window and specify pin name and direction (input/output).

Specify input pins A B VDD GND.

Click Hide and place the pins.
Add output pin $Z$. After you place and wire up the pins and transistor terminals, your schematic should look like this:

**VXL Layout Editor**

Next, you need to invoke VXL. From the NAND2X1 layout editor window, go to: Launch > Layout XL. You will notice that your schematic opens (if not open already) with a Constraint Manager sidebar on the right side.

Now go back to the Virtuoso Layout Editor XL window to create layout view for this schematic. Execute Connectivity > Generate > All From Source… A new window, Generate Layout, will pop up.

Set the different tabs (i.e., Generate, I/O Pins, PR Boundary, Floorplan) as shown below:
All I/O pins are in Metal1 layer (Metal1 dg).

Just as an exercise, if you were to use Metal2 instead for pins A, B, and Z, you would have selected A, B, and Z (hold Ctrl for multiple selection), choose Metal2 drawing layer, and click the Update button.
When done, Click **OK**.

The initial pin and transistor placement in layout will look like this:
The transistors and pins are shown outside a bounding box, which is an estimate of the optimum size of the final layout. Automatic router will use the bounding box to constrain all routing to occur within the box. The bounding box may need to be resized to accommodate all components. An important concept to keep in mind during resizing is that standard cells typically have fixed height (so that power/ground rails line up correctly for routing purposes).

VXL and gpdk090 allow us to create stacked transistors with shared source/drain areas. Zoom in to two transistors on the bottom (to zoom in, type `z` and draw a box around the transistors). Click on the transistor on the top and type `m` to move the object. As you start moving the object, fly-lines indicating connectivity will appear as shown below.

Drag the transistor left and up.

When the source/drain areas are overlapped, left-click to fix the position.

You should see a transistor stack with shared source/drain areas like this (depending on how far you move, you may need to move left/right a bit):
This is a nice NMOS stack for the NAND gate. As you can see, the source/drain contacts have disappeared thanks to VXL.

Back to the big picture, zoom to fit (press ‘F’) and select two NMOS transistors (hold left mouse button and put a virtual box around) and move them over inside the bounding box:
Let’s do the same exercise for the PMOS transistors.

Zoom in to two transistors on the bottom (to zoom in, type `z` and draw a box around the transistors). Click on the transistor on the right and type `m` to move the object. As you start dragging the object to the left, fly-lines indicating connectivity will appear as shown below.

Drag the transistor to the right:

The PMOS transistors do have shared drain contacts because they work in parallel. Connectivity information is extracted from schematic by VXL. The pull-up network looks like this:
Now we remove the boundary that was automatically placed (light blue) (choose it and press ‘delete’), and place a prBoundary rectangle similar to Tutorial 3 (Choose prBoundary drw layer, create a rectangle, and edit the properties by choosing the rectangle and pressing ‘q’), with the following coordinates:
As in the inverter case (INVX1 cell), standard cell height will be 3.6µm, with the power rails extending by 0.3µm over the top/bottom edges.

Bring all the components within the `prBoundary` boundary and add the `Nwell` 1.8µm x 1.8µm in size that extends over the top edge by 0.3µm. Select the PMOS transistors and move them a bit to the right or left (so that fly-lines appear) and make sure Poly lines won’t cross during routing. Your layout should look like this:

Add the power rails (you can draw rectangles or use Create Path command, review *Tutorial 3*, section about Wiring).

In addition to the traditional method of wiring shown in Tutorial 3, you can take advantage of the wiring options of Cadence 6 (`Create > Wiring > Wire`). The mechanics of placing these wires is identical to creating paths, except highlighted fly-lines help you out and the tool can help in identifying different layers (e.g., Poly, Metal1, etc) to make your task easier. (See picture below).
You also need to add M1_PSUB and M1_NWELL contact vias for GND and VDD regions similar to Tutorial 3. For this we set all the enclosures to 0.06 and used 1 row and 4 columns.

Completely wire up the layout.

Continue until you finish routing all the signals. Move VDD and GND pins into the power rails. As you are moving the pins around, notice the fly-lines that indicate the connections.

Before place and route of I/O pins and adding pin labels, your layout should look like this:
Wire up the pins such that an input pin is aligned to \( Z \) vertically (for simple cell-to-cell routing), and the other input is aligned to \( Z \) horizontally.

**Note:** if you are using the wiring option, if at a certain place there are multiple layers are present (e.g., Poly and M1 when connecting I/O pins), following window will ask you which path you would like to create.

Make an appropriate selection, based on which wire you would like to draw.
Your layout should look like this:

One more things before we are ready to verify DRC and LVS:
- label pins

You can (and should) run DRC regularly to make sure DRC errors are caught and fix fast before they mount to a big number of errors.

**Using the Design Rule Manual (DRM)**
In case you have any DRC errors, and you are not sure about the rules, check the DRM manual:

/usr/public.2/ee115c/cadence-labs/gpdk090_v3.4/docs/gpdk090_DRM.pdf
VXL Layout Editing: Adding Pin Labels in Layout

Finally, let’s add pin labels. We can do this from the Virtuoso XL Layout Editing window by selecting Create > Label or simply using shortcut key ‘l’ (small ‘L’). Since there are no labels yet, we first need to determine which label to put on which pin. The pin labels from the schematic view are used as reference. When you select the pin in the layout view, the same pin will be automatically selected in the schematic view thanks to VXL. Simply read the selection.

Selection of pin Z is demonstrated below in the layout and in the schematic.

Before you place pin labels, first set layout display properties to make the pin names visible. From the layout window, select Options > Display… (Or use the shortcut key ‘e’):

Make Pin Names visible by selecting the Pin Names check box. Click OK.
To create a pin label, type ‘l’ (small ‘L’).

Type pin name in the label field. (specifying multiple pins like in the custom layout of the INVX1 cell from Tutorial 3 won’t work! you have do label pins one by one when using VXL).

Select appropriate label layer (Metal1 drw in this case)

Adjust the Height.

Click OK.

And bring the label to the selected pin area:
Your final **NAND2X1** layout will look similar to the following:

Now, we need to verify our design against layout design rules (DRC) and matching between layout and schematics (LVS).

**Design Verification: Design Rule Check (DRC)**

To perform a Design Rule Check (DRC), select **Assura > Run DRC...** from the **Virtuoso XL Layout Editing** window. The DRC form appears:
Make sure the **Rules File** is set to following:

/usr/public.2/ee115c/cadence-labs/gpdk090_v3.4/assura/drc.rul

Click **OK** to run DRC. You can monitor progress of the DRC run using the progress window. When the run is complete, following pop-up dialog appears:

Click **Yes** to see the results.
If you followed the instructions and DRC rules, your design should be DRC clean!

The next step in the verification process is layout versus schematic check. Before doing that, close the DRC run from Assura > Close Run.

**Design Verification: Layout Versus Schematic (LVS) Check**

To start Assura LVS run, go to Assura > Run LVS... Following window will appear:

Make sure Extract Rules and Compare Rules files are set to following values, respectively:

/usr/public.2/ee115c/cadence-labs/gpdk090_v3.4/assura/extract.rul
/usr/public.2/ee115c/cadence-labs/gpdk090_v3.4/assura/compare.rul
Click **OK** to start the LVS run. If you get the following pop-up message:

Click **OK** to continue.

If you paid close attention to flylines in the layout and their correspondence to objects in the schematic, your effort will rewarded with the following message:

You can choose **Yes** to see the LVS Debug window.

The debug window:

**CONGRATULATIONS! Your design is LVS-clean!**
Close the LVS run from Assura > Close Run.

**Finishing Cell - Symbol View**

We are getting ready to finish this cell. Let’s create symbol view, which can (and are) used for hierarchical designs in the future. (review symbol view generation from *Tutorial 2*, section *Creating Symbol View*) The most important steps are repeated here for convenience.

In Virtuoso schematic editor, choose Create > Cellview > From Cellview... and select from schematic to symbol view as shown in the pop-up window below.

![Cellview From Cellview](image)

After you click OK, the following window will appear:

![Symbol Generation Options](image)

Modify Pin Specifications to place VDD and GND pins on the top and bottom, respectively. Click OK.
The default box-shaped symbol view is created as shown below:

Modify the symbol shape to represent the typical symbol of a NAND gate. In the Virtuoso Symbol Editing window, go to Create > Shape menu and select needed shapes (you may review Tutorial 2, section Creating Symbol View). Your final symbol view should look something like this:
Click Save and check the CDS.log window. It should display the following message:

“NAND2X1 symbol” saved.

This completes the design of a 2-input NAND gate. NAND2X1 cell is ready for use in hierarchical schematic and layout.

### Layout Editing: Useful Commands

Some useful layout commands are summarized below:

#### Zooming

There are several methods for zooming found in the View menu.

- One easy way to zoom to the exact region you want is by using the zoom hot key. Type ‘z’. This puts you in zoom mode. Note that the cursor has changed. Next hold down the left mouse button and "drag" out a box which surrounds the region you wish to zoom to.
  
  When you release the mouse the screen will zoom to where your box was.

- The hotkey Shift-z can be used to zoom out by a factor of two.

- The hotkey Ctrl-z can be used to zoom in by a factor of two.

- If you mess up don't panic. Remember, ‘f’ always zoom to fit.
Selecting and Moving Layout
When Virtuoso is in main mode (the default), if you simply drag out a region while holding down the left mouse button, whatever is within the box will be selected when you release the button and will be highlighted in white. Drag a box over the stacked nfet's we just drew. When you release the mouse button, whatever is "selected", in this case the fet cell, will be highlighted.

Once you have selected an object or paint you can do lots of things with it.
- For example you can move it by typing the ‘m’ hot-key.
  You can move layout up/down/left/right one grid at a time by clicking at the selection and moving the mouse. Try it.

You can also select objects or paint by clicking on them.
- Clicking the left mouse button once on a piece of paint selects that particular rectangle of paint.
- Clicking once on a polygon or cell will select the object.

Duplicating Layout, Cut, Copy and Paste
Virtuoso supports Cut, Copy, and Paste in the same format you would see on any good Mac- or PC-based drawing or painting program.

Tip: all of the zoom, move, cut, and paste, rotate, etc. features that we just executed using hot keys also have menu equivalents which can be found in the View or Edit menu.

Other Fun Stuff!!
Virtuoso Layout Suite XL has many options that cannot possibly be covered in short tutorials like this. You are encouraged, if interested, to try these on your own. This is a powerful software that cannot easily be accessed outside this class; take this opportunity to learn as much as you can if you would like to continue in this field.

Some examples include “Reinitialize Floorplan” option that you can use to plan your layout before stating wiring it, “Show/Hide selected incomplete nets”, etc.