Problem 1: Flip-flop timing characterization

a) Create a copy of flip-flop cell DFFQX1 from gsclib090 into your ee216a library. Analyze the circuit, identify main building blocks, and explain the circuit operation.

SOLUTION
This is a standard master-slave flip-flop, as shown below. Slave latch is slight modification of the master design (CMOS master is followed by standard transmission-gate slave). Output buffer isolates internal node of the slave latch and provides necessary drive for the load.

b) Sweep D arrival time with respect to Clk and plot $t_{\text{Clk-Q}}$ time versus D-Clk offset. Find $t_{\text{setup}}$ and $t_{\text{hold}}$ defined as minimum $t_{\text{D-Q}}$. What percentage $t_{\text{Clk-Q}}$ delay increase from the nominal do these definitions of $t_{\text{setup}}$ and $t_{\text{hold}}$ correspond to? Generate two plots: 1→0, 1→0 transitions. Determine corresponding parameters: $t_{\text{setup}}(0)$, $t_{\text{hold}}(0)$, $t_{\text{setup}}(1)$, $t_{\text{hold}}(1)$.

SOLUTION
Simulation setup is made such that both D and Clk inputs are driven from INVX1 inverter, output of the test flip-flop is loaded with D input of another flip-flop. D-Clk arrival time is swept until minimum in D-Clk delay is found. This point is used to derive setup and hold times for logic 0 and logic 1 (shown below).
Problem 2: Data-transition look-ahead flip-flop

a) Consider the flip-flop shown below. Analyze and explain its operation. In particular, explain the functionality of blocks A, B, and C.

**SOLUTION**

This is a data-transition look-ahead flip-flop. Functionality of main blocks is indicated in the figure.
b) When is this circuit useful? Discuss its key advantages and disadvantages.

**SOLUTION**

This is the Data-Transition Look-Ahead Latch (DTLA-L) by Nogawa and Ohtomo [1]. It is a non-inverting Pulsed-Latch type of flip-flop. The text below is borrowed from Digital System Clocking book [2].

**Circuit Operation:** The Data-Transition Look-Ahead (DL) circuit performs an XNOR function on D and Q. When $D = Q$, the DL circuit produces a logic “0” at $P_1$ and generation of the internal clock $\{CP, \overline{CP}\}$ is disabled. When $D \neq Q$, $P_1$ is “low” and the clock control (CC) circuit enables generation of $\{CP, \overline{CP}\}$.

The Pulse Generator (PG) circuit generates a short pulse CPI at each rising edge of the external clock Clk. Internal clock pulse CP then triggers the Latch if $D \neq Q$. The PG is essential for the operation of the Latch. If there was no pulse generator, this Latch could be triggered by data instead of the clock. For example, if $D \neq Q$ and the rising edge of CPI arrives, then the clock pulse CP is generated and Q changes. However, if $D$ changes again while the clock is still high and becomes different from Q, then another pulse of internal clock CP would be generated and the CSE would be actually triggered by the data.

**Analysis of DTLA-L:** In order to evaluate the benefit of clock gating, it is essential to find the energy overhead associated with internal clock gating circuitry. For that purpose, a portion of DTLA-L circuit shown in Fig. 8.21 is analyzed.

*Fig. 8.21: DTLA-L without gating.*
When the energy-per-transition of the circuit in Fig. 8.20 is subtracted from the energy-per-transition of the circuit in Fig. 8.21, the energy overhead in data look-ahead, clock control and pulse generator is obtained. This only applies to 0-1 and 1-0 input transitions, because only then are all sub-circuits in Fig. 8.20 and Fig. 8.21 active. For 0-0 and 1-1 input transitions, the internal clock (shaded inverters) is activated in the circuit of Fig. 8.21, and deactivated in the circuit in Fig. 8.20.

The PG is commonly shared among several Latches, so further energy breakdown is needed to understand where the energy goes exactly. Energy consumed by the PG is estimated by simulation of a stand-alone PG loaded with capacitance $C_{in(CC)}$ that CPI “sees” when “looking” into the CC circuit as shown in Fig. 8.22. The PG consumes energy regardless of what input transition occurs. The portion of the PGs energy dissipation is attributed to each CSE through external clock energy parameter.

![Pulse Generator](image)

**Fig. 8.22: Pulse generator.**

**Energy efficiency of DTLA-L:** Energy saving capabilities of DTLA-L depend on two parameters: 1) number of Latches, $N$, driven by a single PG, and 2) input data transition probability. The energy consumed per Latch during one clock cycle, when $D = Q$ is given by:

$$E_{D-idle} = E_{0-0} = E_{1-1} = \frac{E_{PG}(N)}{N} + E_{Cin}$$  \hspace{1cm} (8.1)

The energy consumption when $D$ undergoes a 0-1 or 1-0 transition is given by (8.2)-(8.3).

$$E_{0-1} = E_{D-idle} + E_{CLK} + E_{DL+CC} + E_{int} + E_{ext}$$  \hspace{1cm} (8.2)

$$E_{1-0} = E_{D-idle} + E_{CLK} + E_{G} + E_{int}$$  \hspace{1cm} (8.3)

**Comparison with M-S Latch:** Assuming there is no glitching at input $D$, probability of 0-1 and 1-0 transitions is equal: $\alpha_{0-1} = \alpha_{1-0} = \alpha/2$, where $\alpha$ is data transition probability. Under this postulation, average energy consumption of the DTLA-L and the conventional M-S Latch CMSL are:

$$E_{DL-DF} = \frac{\alpha}{2} \cdot (E_{0-1} + E_{1-0}) + \frac{1-\alpha}{2} \cdot E_{D-idle}$$  \hspace{1cm} (8.4)

$$E_{MSL} = \frac{\alpha}{2} \cdot (E_{0-1} + E_{1-0}) + \frac{1-\alpha}{2} \cdot E_{CLK} + E_{Cin}$$  \hspace{1cm} (8.5)

In Equation (8.5), $E_{Cin}$ is the energy consumed in switching $C_{in}(CLK)$ of the MSL. This term represents the energy consumed by a simple clock buffer that drives $C_{in}(CLK)$ and is included for a fair comparison with the DTLA-L where $E_{PG}(N)/N$ represents the energy consumption in PG per Latch.

Figure 8.23 shows comparison of energy consumption in DTLA-L and MSL as a function of $N$ and $\alpha$. The figure shows that DTLA-L has better energy efficiency than the MSL for $N > 2$ and $\alpha < 0.25$. 
Fig. 8.23: Energy comparison of DTLA-L and CMSL (similar to the one in Prob.2).

**Pros:** low energy at very low activity.

**Cons:** long delay, large area.

**References:**