Power/Clock Distribution and Floorplanning

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Slides: Courtesy of Prof. Dejan Marković

UCLA

Power Distribution
**Power = ...**

- **Routing resources**
  - 20-40% of all metal tracks used by Vdd, Gnd
  - Increased power → denser power grid

- **Pins**
  - Vdd or Gnd pin carries 0.5-1W of power
  - Pentium 4 uses 423 pins: 233 Vdd or Gnd
  - More pins → higher cost package
    (+ package development, board design...)

- **Battery cost**
  - 1kg NiCd can power P4 for <1hr

- **Performance**
  - High chip temperature degrades performance
  - Large across-chip temp variations induce clk skew
  - High chip power limits use of high-perf circuits
  - Power transients determine min supply

*Courtesy: A. Kahng*

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**Power = Package**

- **Pentium 4 die is about 1.5g and less than 1cm^3**
- **Pentium-4 in package with interposer, heat sink, and fan can be 500g and 150cm^3**

![Package Diagram](image)

Modern processor packaging is complex and adds significantly to product cost.

*Courtesy: A. Kahng*
Packaging

- **Package functions**
  - Mechanical connection of chip to board
  - Electrical connection of signals and power from chip to board with very little delay or distortion
    - Short wires with low R and L
  - Removes heat produced on chip and thermal expansion and stress
  - Protects chip from mechanical damage
  - Inexpensive to manufacture and test

- **Main issues:**
  - Cost
  - Thermal impedance: how effectively package removes heat from the die
  - Lead inductance
    - Ceramic pin grid array package – lowest
    - Cheap epoxy plastic – highest

  [Reading: Weste, Harris VLSI book]

Package Types

- **Through-hole vs. surface mount**
Multi-Chip Modules

- Pentium Pro MCM
  - Fast connection of CPU to cache
  - Expensive, requires known good dice

Concept of a Typical Chip Package
### Chip-to-Package Connections

- Traditionally, chip is surrounded by **pad frame**
  - Metal pads on 100 – 200 μm pitch
  - Gold **bond wires** attach pads to package
  - **Lead frame** distributes signals in package
  - Metal **heat spreader** helps with cooling

![Chip-to-Package Connections Diagram]

### Figure out Pin Locations (PCB Routing)

- **120 pins**
  - chip: 3.5mm²

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<thead>
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<th></th>
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- **Ceramic PGA**
  - SSM P/N CPG12028 (~ $30)

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- **Test socket**
  - YAMAICHI NP89-19601-KS11730 (~ $70)

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**Advanced Packages**

- Bond wires contribute parasitic inductance
- Fancy packages have many signal, power layers
  - Like tiny printed circuit boards
- **Flip-chip** places connections across surface of die rather than around periphery
  - Top level metal pads covered with solder balls
  - Chip flips upside down
  - Carefully aligned to package (done blind!)
  - Heated to melt balls
  - Also called C4 (Controlled Collapse Chip Connection)

**Package Parasitics**

- Use many $V_{DD}$, Gnd in parallel
  - Inductance, $I_{DD}$
Heat Dissipation

- **Comparison**
  - Light bulb: 60W, surface area ~120cm² (too hot to touch)
  - Itanium 2: 130W, die area ~4cm² (60x higher power density)

- The heat flows from the transistor junctions through the substrate and package
  - Can be spread across a heat sink,
  - Then carried away through the air by convection
  - Liquid cooling used in extreme cases ($$$)

- **Analogy**
  - Current flow: voltage difference / resistance
  - Heat flow: temperature difference / thermal resistance

Thermal Resistance

- \[ \Delta T = \theta_{ja} \cdot P \]
  - \( \Delta T \): temperature rise on chip
  - \( \theta_{ja} \): thermal resistance of chip junction to ambient
  - \( P \): power dissipation on chip

- Thermal resistances combine like resistors
  - Series and parallel

- \( \theta_{ja} = \theta_{jp} + \theta_{pa} \)
  - Series combination
Thermal Impedance

- Ceramic pin-grid arrays – 15 to 30 °C/Watt
- Plastic Quad Flat Packs – 40 to 50 °C/Watt
- Heat dissipation:
  - Finned heat sinks
  - Embedded metal slugs
- High-cost packages:
  - Forced air or liquid cooling through package ducts
  - Example: IBM Thermal Conduction Module

Example: Thermal Resistance and Power

- Your chip has a heat sink with a thermal resistance to the package of 4.0°C/W
- The resistance from chip to package is 1°C/W
- The system box ambient temperature may reach 55°C
- The chip temperature must not exceed 100°C
- What is the maximum chip power dissipation?
Power Distribution

- **Power Distribution Network functions**
  - Carry current from pads to transistors on chip
  - Maintain stable voltage with low noise
  - Provide average and peak power demands
  - Provide current return paths for signals
  - Avoid electromigration & self-heating wearout
  - Consume little chip area and wire
  - Easy to lay out

Power Supply Drop/Noise

- **Supply noise is variations in power supply voltage that manifest as noise onto the logic gates**
  - Power supply wiring resistance creates voltage variations with current surges
  - The current surge for static CMOS depend on dynamic behavior of circuit

- **Tackling the drop**
  1. \( V_{DD}-GND \) capacitance
     - Based on total maximum switched capacitance (10x)
  2. Redesign power/ground network to reduce resistance.
     - Based on maximum current required by each block
  3. Adjust activity to another clock cycle to reduce peak current.
     - Scheduling
Power Requirements

- $V_{DD} = V_{DDnominal} - V_{droop}$
- Want $V_{droop} < +/- 10\%$ of $V_{DD}$
- Sources of $V_{droop}$
  - IR drops
  - $L \frac{di}{dt}$ noise
- $I_{DD}$ changes on many time scales

![Power vs Time Diagram]

Issue #1: RI Introduced Noise

![Circuit Diagram]
Power IR Drop Example

Drive a 32-bit bus, total load of each wire: 2pF, 
\( R = 0.125 \Omega/\text{square} \), want delay \( \sim 0.5 \text{ns} \), < 10% drop
- \( R \) for each transistor needs to be < 0.25k\( \Omega \)
  - To meet \( RC = 0.5 \text{ns} \)
  - Effective \( R \) of bits together is 250/32 = 7.5\( \Omega \)
  - For < 10% drop, Power R must be < 1\( \Omega \)
  - That is only 8 squares

Must support Total Power
- Chips today dissipate 5-50W
- Implies total current is 4-40A (Power = IV)
  - Supply is now as low as 1.2V!
  - Very big problem currently
  - Use many supply pins (@0.2mA each), and wide wires for low R
  - Grids of higher level metal for power is a must!
    - Thicker metal... lower R

Issue #2: \( \frac{dI}{dt} \)

Impact of inductance on supply voltage
- Change in current induces the change in voltage
- Longer supply lines have larger \( L \)
**L di/dt: Example**

- (12.3.3 W&H) A 1GHz chip transitions from idle (20 A) to full power (60 A) operation in a single cycle. If the power supply has 20 pH of series inductance, estimate the power supply noise caused by this transition if the chip has no internal bypass capacitance.

**Design Techniques to Address L di/dt**

- Separate power pins for I/O pads and chip core
- Multiple power and ground pins
- Position of power and ground pins on package
- Increase $t_r$ and $t_f$
- Advanced packaging technologies
- Decoupling capacitances on chip and on board
**Bypass Capacitors**

- Need low supply impedance at all frequencies
- Ideal capacitors have impedance decreasing with $\omega$
- Real capacitors have parasitic $R$ and $L$
  - Leads to resonant frequency of capacitor

**Frequency Response**

- Use multiple capacitors in parallel
  - Large $C$ near regulator has low impedance at low frequencies
  - But also has a low self-resonant frequency
  - Small capacitors near chip and on chip have low impedance at high frequencies
- Choose caps to get low impedance at all frequencies
Decoupling Capacitors

Decoupling capacitors are added:
- On the board (right under the supply pins)
- On the chip (under the supply straps, near large buffers)

On-chip Decoupling Capacitance

- Static CMOS logic dynamically switches (no dc current)
  - Supply just need to provide the average current
  - Peak current needs to come from nearby capacitance

- Basically the same as charge sharing
  - Use $C_{\text{decoup}} > 10 \times C_{\text{switched}}$ to guarantee $< 10\%$ $V_{DD}$ drop
  - Put capacitance near load with little resistance
    - Disseminate the capacitance throughout the standard cell
    - The more the merrier
    - Part of the P&R tool
Power System: Lumped Model

- Power comes from regulator on system board
  - Board and package add parasitic $R$ and $L$
  - Bypass capacitors help stabilize supply voltage
  - But capacitors also have parasitic $R$ and $L$
- Simulate system for time and frequency responses

Power Distribution Strategy

- Low-level distribution is in Metal 1
- Power has to be “strapped” in higher layers of metal
- The spacing is set by IR drop, electromigration, inductive effects
- Always use multiple contacts on straps
**Power and Ground Distribution**

(a) Finger-shaped network  
(b) Network with multiple supply pins

**Top-Level Power and Gnd Routing**

- Usually on the top layer of metal, and then distributed to the lower levels
Electromigration (1)

Limits dc current to 1mA/μm

Electromigration (2)
Power and Clock Lines: Sizing

- Check for metal migration at worst power corner
- Do the following checks:

<table>
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<tr>
<th>PROCESS</th>
<th>TEMP</th>
<th>VOLTAGE</th>
<th>TESTS</th>
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<tbody>
<tr>
<td>Fast-n/fast-p</td>
<td>0°C</td>
<td>5.5V (3.6V)</td>
<td>Power dissipation (DC), clock races, hold time constraints</td>
</tr>
<tr>
<td>Slow-n/slow-p</td>
<td>125°C</td>
<td>4.5V (3.0V)</td>
<td>Circuit speed, setup time constraints</td>
</tr>
<tr>
<td>Slow-n/fast-p</td>
<td>0°C</td>
<td>5.5V (3.6V)</td>
<td>Pseudo-nMOS noise margin, level shifters, memory write/read, ratioed circuits</td>
</tr>
<tr>
<td>Fast-n/slow-p</td>
<td>0°C</td>
<td>5.5V (3.6V)</td>
<td>Memories, ratioed circuits, level shifters</td>
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</tbody>
</table>

Power Supply Rules

- The exact rules depend on the technology
  - Each technology file should have its rules for resistance and electromigration
- Example Rules:
  - Must have a contact for each 16\(\lambda\) of transistor width (more is better)
  - Wire must have less than 1mA/\(\mu\)m of width
  - Power/Gnd width = Length of wire \(\times\) Sum (all transistors connected to wire) / \(3 \times 10^6\lambda\) (very approximate)
- For small designs, power supply design is less of an issue
  - Total power is small
  - Chip is small, so wires are short
    - Will not be an issue in this class
Working with Scaled $V_{dd}$

- Additional power/gnd pads, level shifter

**Simple On-chip Level Converter**

<table>
<thead>
<tr>
<th>VddL (V)</th>
<th>tp:0-1 (ps)</th>
<th>tp:1-0 (ps)</th>
<th>tp:avg (ps)</th>
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<td>0.4</td>
<td>1725</td>
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<td>1738</td>
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<td>435</td>
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<td>408</td>
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<td>0.9</td>
<td>98</td>
<td>695</td>
<td>396</td>
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<tr>
<td>1.0</td>
<td>86</td>
<td>693</td>
<td>389</td>
</tr>
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</table>
Example: $V_{DDL} = 0.4V$

Clocking Issues:
Distribution, Energy
Clock Distribution

- **Goals:**
  - Deliver clock to all memory elements with acceptable skew
  - Deliver clock edges with acceptable sharpness

- Clock network design is another one of the big challenges in the design of a large chip

- Clocks are generally distributed via wiring trees

- Want to use low-resistance interconnect to minimize delay

- Use multiple drivers to distribute driver requirements
  - Use optimal sizing principles to design buffers
  - Clock lines can create significant crosstalk

Issues in Clock Distribution Network

- **Skew**
  - Process, voltage, temp.
  - Data dependence
  - Noise coupling
  - Load balancing

- **Power, CV²f – (no ½ or α)**
  - Clock gating

- **Flexibility/Tunability**
  - Compactness
  - fit into existing layout/design

- **Reliability**
  - Electromigration

See videos from P. Restle (IBM) on classwiki
**Clock Distribution Methods**

- **RC-Tree**
  - Less capacitance
  - More accuracy
  - Flexible wiring

- **Grids**
  - Reliable
  - Less data dependency
  - Tunable (late in design)

Shown here for final stage drivers driving F-F loads

---

**RC Trees, Clock Distribution**

- Observe: only relative skew is important

- **H-Tree**
- **X-Tree**
- **Binary-Tree**

Asymmetric trees that match RCs can be used

H-Tree Network
More Realistic H-Tree

[Restle98]

The Grid System

- No RC-matching
- Large power

DEC Alpha Examples

21064  21164  21264
Examples of Distribution

H-Tree
Asymmetric RC-Tree
- IBM

Grids
DEC [Alphas]

Serpentines
Intel x86
[Young ISSCC97]


Single-phase clocking

2 distributed driver channels
- Reduced RC delay/skew
- Improved thermal distribution
- 3.75 nF clock load
- 58 cm final driver width

Local inverters for latching

Conditional clocks in caches to reduce power

More complex race checking

Device variation
Example: EV6 (Alpha 21264) Clocking (1998)

600MHz, 0.35μm CMOS

- Multiple conditional buffered clocks
  - 2.8 nF clock load
  - 40 cm final driver width
- Reduced load/skew
- Reduced thermal issues
- Multiple clocks complicate race checking

Global clock waveform

EV6 Clock Results

GCLK Skew
(at V_{DD}/2 Crossings)

GCLK Rise Times
(20% to 80% Extrapolated to 0% to 100%)

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**Intel Processors**

<table>
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<th>Pentium® III</th>
<th>Pentium® 4</th>
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<td>April 2000</td>
<td>Dec 2001</td>
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<td>2GHz</td>
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<tr>
<td>Pipeline Stages</td>
<td>12/14</td>
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<td>22/24</td>
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<td>24M</td>
<td>42M</td>
</tr>
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<td>16K/16K/-</td>
<td>16K/16K/256K</td>
<td>12K/8K/256K</td>
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<td>0.25µm, 4M</td>
<td>0.18µm, 6M</td>
<td>0.18µm, 6M</td>
</tr>
<tr>
<td>Max Power</td>
<td>27W</td>
<td>23W</td>
<td>67W</td>
</tr>
</tbody>
</table>

- **Increasing clock speeds and die size**
  - Balancing skew using simple RC trees becoming less effective
- **Insertion delay 7-8FO4 due to increased die**
  - Clock skew control harder to due to increasing PVT variations
- **Use of active deskewing circuits**

**Some Energy Reduction Ideas**

- **Clock gating**
  - Global
  - Local

- **Low-swing clocking**
  - Reduced-swing Clk drivers
  - CSE redesign
  - N-only CSE w/ low-swing Clk

- **Dual-edge triggering**
  - Latch-mux
  - Pulsed-latch
**Global Clock Gating**

- Used to save clocking energy when data activity is low

(a) Nongated clock circuit, (b) gated clock circuit.
[Kitahara et al. 1998]

**Low-Swing Clocking: Driver Re-design**

- Half-swing clock drivers: 50% power reduction (minus some penalty in clock drivers)

[Kojima at al. 1995]
N-only Clocked Latches

- Bring clock only to n-MOS transistors to allow reduced clock swing without conflict with partially turned-off p-MOS transistors
- Reduced clocking energy with some penalty in performance
  - $Clk$ is in the critical path

(a) conventional TG MSL, (b) pulsed-latch

Dual-Edge Triggering (DET): Latch-Mux

- Saves clocking energy *regardless* of data activity!
- Extra Mux $\rightarrow$ longer delay
DET Latch-Mux: Circuit Example

- Pass-gate latches
  - One transparent when \( Clk = 0 \)
  - One transparent when \( Clk = 1 \)
- Pass-gate multiplexer that selects the output of the opaque latch

\[ \text{[Llopis and Sachdev, 1996]} \]
Floorplanning: Overview

**Introduction:** With ever larger designs, it is increasingly important to plan a design at an early stage. This early plan helps constrain later design decisions in terms of area, wire usage, ports, and port locations. The early stage plan, a.k.a. a **floorplan**, is fleshed out with increasing details with the design flow. The issue is a chicken-and-egg problem in that an accurate **floorplan** is difficult without knowing the details, and yet, building the details is greatly facilitated with a **floorplan**. So such a plan is a first guess. We use a lot of estimates for area to arrive at a reasonable plan. The plan discussed in this lecture includes area for blocks, ports and their locations, routing channels, metal layer usage, power and ground routing, clock routing, and I/O pins. The result is a diagram of the chip...

---

Design Flow: Floorplanning

```
READ TARGET LIBRARIES
READ HDL FILES
ELABORATE DESIGN
SET TIMING AND DESIGN SPECS
SYNTHESIZE DESIGN
ANALYZE TIMING
MEET SPECS?
   NO
   YES
   Floorplan

PLACE AND ROUTE
EXTRACT PARASITICS

Area, Timing, Power Report

---------- TypicalLib
---------- Top.v

---------- Top.enc_setups.tcl
---------- Top.place, Top.route
```
Floorplanning

- This is a plan of the chip,
  - Shows the module/blocks
  - The space needed for wires
    - In a cell it is called the “color plan”; at the chip level - “floorplan”
- How \( V_{DD}, V_{GND} \), and Clock are distributed + wire width
- The area is estimated by the type of block (dpath or ctrl)
- The routing is based on position of I/O pins of each block
  - Floorplanning tools will help position large blocks, rotating, flipping to minimize the routing between blocks
  - Helps predict wiring loads and area of chip
  - Makes sure you have enough pins, and space
- Early in design
  - Floorplan budgets area, wire area/delay. Negotiate tradeoffs
- Late in design
  - Make sure the pieces fit together as planned
  - Implement the global layout

Floorplanning

- Input
  - Required
    - Design netlist
    - Area requirements
    - Power requirements
    - Timing constraints
    - Physical partitioning information
    - Die size vs. performance tradeoff
  - Optional
    - I/O placement
    - Macro placement information
- Output (design ready for standard cell placement)
  - Die/block area
  - I/Os placed
  - Macros placed
  - Power grid designed
  - Power pre-routing
  - Standard cell placement areas
Floorplanning Output

A Conceptual Floorplan

- Blocks inside a pad frame
- Routing may be inside blocks but need to interconnect them
- Brick and Mortar
  - Random sized blocks that are more difficult than standard cell rows to route
- Layout hierarchy not deep
  - Tough to do this too many times
Example Chip Layout

More Complex Chip
Design Flow and Physical Design Stage

- **Definitions:**
  - **Cell**: a circuit component to be placed on the chip area. In placement, the functionality of the component is ignored.
  - **Net**: specifying a subset of terminals to connect several cells.
  - **Netlist**: a set of nets which contains the connectivity information of the circuit.

Placement

- **Input**
  - A set of cells and their complete information (a cell library)
  - Connectivity information between cells (netlist information)
- **Output**
  - A set of locations on the chip, one location for each cell
- **Goal**
  - The cells are placed to produce a routable chip that meets timing and other constraints (e.g. low-power, noise, etc.)
- **Challenge**
  - The number of cells in a design is very large (> 1M)
  - The timing constraints are very tight
Placement Problem

A bad placement

A good placement

Courtesy: Andrew Kahng, UCSD

Placement Footprints

- Standard cell
- Data path
- IP – floorplanning

Courtesy: Andrew Kahng, UCSD
Placement Footprints

Reserved areas

Core
IO
Control

Mixed Data Path & sea of gates:

Courtesy: Andrew Kahng, UCSD

Unconstrained Placement

Courtesy: Andrew Kahng, UCSD
Floorplanned Placement

Placement: Blocks and Wires

- **Placement**
  - Simple: min length of wires
  - Timing-driven: cost of wires weighted to min critical-path delays

- **Blocks**
  - Blocks have area and aspect ratio
  - Different rotations and reflections
  - Uniform size blocks are easier to interchange

- **Wires**
  - Cannot ignore wiring during block placement
    - Large wiring areas may force rearrangement of blocks
  - Wiring plan must consider area and delay of critical signals
  - Blocks divide wiring area into routing channels

- **Next step: routing**
  - Design saved in standard design exchange format (DEF) for routing
Hierarchical Partitioning

- Levels of partitioning
  - System-level
    - Each sub-system can be designed as a single PCB
  - Board-level
    - Circuit assigned to a PCB is partitioned into sub-circuits each fabricated as a VLSI chip
  - Chip-level
    - Circuit assigned to the chip is divided into manageable sub-circuits

Courtesy: Andrew Kahng, UCSD

Delay at Different Levels of Partitions

Courtesy: Andrew Kahng, UCSD